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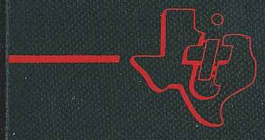

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Louis A. Delhom
Senior Engineer
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To my mother and father

Design and Application of Transistor Switching Circuits

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Preface

Basic principles of transistor operation and certain aspects of transistor circuit design are taught in many courses offered by engineering colleges, technical schools, and industry. The author feels, however, that many of the finer details of transistor switching-circuit design are often omitted from these courses. An attempt is made here to discuss important characteristics of switching transistors and to relate certain features of circuit operation to these characteristics. Stated more simply, one object of this book is to present a straightforward approach to the design of transistor switching circuits.

Numerous circuit configurations of the active transistor, together with inactive elements such as resistors and diodes, give predictable output signals for certain *combinations* of input signals. These circuits are classified as "logic circuits" and are widely used in computer systems and in digital control systems. A second purpose of this book is to describe circuit organization and circuit design of several basic logic elements.

Various active semiconductor devices are included in the category of "transistor." Among these are the point-contact transistor, the bipolar transistor, the unijunction transistor, and the field-effect transistor. The bipolar transistor, which is the designation given to the various junction transistor structures, is by far the most widely used of all transistor types. This bipolar transistor is so named because its operation depends upon the flow of both positive and negative charges within the device. The bipolar transistor is usually referred to simply as a transistor, whereas the other three types are generally identified by their full names. Only the bipolar transistor is considered in this book; the device is hereafter referred to as a transistor.

It is assumed that the reader understands the basic mechanism of transistor operation, i.e., the concept of hole and electron flow through N- and P-type semiconductors. The material of Chap. 1 elaborates upon this concept and forms the basis for much of the analysis of succeeding chapters. Chapter 2 shows the manner in which physical characteristics of the transistor determine certain ac parameters of the device; a small-signal equivalent circuit of the transistor is presented. Various types of low- and medium-power switching transistors are then discussed in Chap. 3. Chapter 4 presents a detailed discussion of the transistor as a switch. A discussion and explanation of the transistor data sheet is given in Chap. 5. These five chapters form a background for the design of transistor switching circuits.

Sufficient material is presented in the above chapters to allow a description of

circuit design for various saturated-transistor stages; Chap. 6 presents design details for this important class of transistor switching circuits.

The technique of graphical circuit analysis is presented in Chap. 7; this provides a background for certain material in Chaps. 8 and 11.

A nonsaturated logic circuit, the emitter-follower, is described in Chap. 8. This circuit is widely used as an impedance transformer.

Transistor switches, often in conjunction with diodes, are frequently used as logic elements. Chapter 9 presents a discussion of logical operations and shows how switches can be used to implement logic functions. The use of transistors and diodes as logic elements is presented in Chap. 10.

The remaining four chapters present more specialized circuit types than those already described. Nonsaturated switching circuits are described in Chap. 11. Chapter 12 presents a description of flip-flop circuits, and Chap. 13 shows how this circuit type can be used in registers and counters. Diode decoders, which are a necessary part of many counter networks, are also described in Chap. 13. Transistor switching circuits may be used to generate and to shape pulses; Chap. 14 describes circuits which perform these functions.

A rather subtle influence has been exerted on the content of this book by the author's own experience in the semiconductor industry, including various discussions with many of his colleagues. The author is particularly indebted to William Nunley and Roger Webster for explaining several points on transistor fabrication and the properties of epitaxial transistors, respectively.

Louis A. Delhom

Contents

1

Transistor Physical Characteristics

1-1. INTRODUCTION

A designer of transistor switching circuits can consider the transistor as a four-terminal network which has certain input and output characteristics, including a known relationship between input signals and output signals. These characteristics can be obtained by making measurements at the transistor terminals and may be displayed as plots of currents and voltages or listed as impedance, admittance, or hybrid parameters.[1,*] A knowledge of these characteristics, in addition to information concerning allowable maximum ratings of voltage, current, and power dissipation, usually enables the designer to specify circuit configurations and component values which give electrical networks that fulfill operating requirements. However, many transistor circuits do not perform as predicted by a design based exclusively on the characteristics described above. In order to anticipate causes of poor switching-circuit operation and thus consider these factors as the circuit is designed, it is necessary to have a thorough understanding of those principles of transistor operation which are of particular importance in transistor switching circuits.

This chapter presents a discussion of certain aspects of transistors which are relevant to the design of transistor switching circuits. The approach used here to study the important characteristics of switching transistors is first to discuss the junction transistor. Strictly speaking, all transistors described in this book are junction transistors; however, as used here, the term "junction transistor" implies either the grown-junction or alloy-junction transistor type. These devices, which were developed after invention of the point-contact transistor, are the predecessors of most present-day transistor types. The newer devices have largely resulted from research directed at improving certain electrical characteristics of the early junction transistors. Higher operating frequency and larger dynamic range over that of the original junction structures are two features of some of the newer devices.

Because the junction transistor is the least sophisticated of all transistor types, a study of transistor operation usually begins with this type. Operation of advanced

* Superscript numbers indicate items listed in References at the end of the chapter.

transistor types is explained by extending or modifying the theory of operation for the junction device. A classic paper by Ebers and Moll[2] has served as a foundation for many subsequent papers directed toward an analysis of the junction transistor,* and much of the material of this chapter is based upon their results.

Because of its simple geometry, the grown-junction transistor is used for illustration in this chapter. Certain dc parameters of the transistor are shown to be determined by its physical characteristics, which include base width as well as resistivity of the emitter, base, and collector regions.

Although transistors may have either the N-P-N or P-N-P structure, the discussion throughout this book of transistor principles and circuits is usually concerned with the N-P-N type. In order for an analysis to hold for the P-N-P transistor, or complementary device to the N-P-N type, the input- and output-signal levels should be shifted, and different bias conditions should be employed; the roles of electrons and holes should be interchanged for those portions of the text where analysis is in terms of these two quantities.

A large number of equations is to be presented throughout the book. The sign convention is given now in order to avoid confusion later. The various circuit diagrams show actual directions of current flow. Equations derived from these figures reflect the relative polarities of voltage levels, and, except where noted, the signs associated with an equation are correct if the absolute value of each term is substituted into the equation.

1-2. COMMON-BASE FORWARD CURRENT GAIN

Figure 1-1 shows an N-P-N grown-junction transistor operated as a grounded-base device. Because the base terminal is common to both input and output circuits, this transistor connection is also referred to as a "common-base configuration." The transistor is seen to be biased so that the emitter-base diode is forward-biased and the collector-base diode is reverse-biased. Basic transistor theory teaches that under these bias conditions, electrons flow from the emitter into the base region, and holes flow from the base into the emitter material.[3] These two types of carrier flow are designated in the figure as I_N and I_P, respectively. Conventional current flow in the emitter external circuit is shown as I_E and is the

* Ebers and Moll present two equations which completely characterize the junction transistor; external current-voltage relationships of the transistor are then related to these equations. In addition, an excellent discussion is given of certain transistor parameters which affect voltage drops, leakage currents, and switching times of the junction transistor. Although the paper deals specifically with the alloy-junction transistor, much of the material applies, in general, to other transistor types. For this reason, the work remains a basic reference.

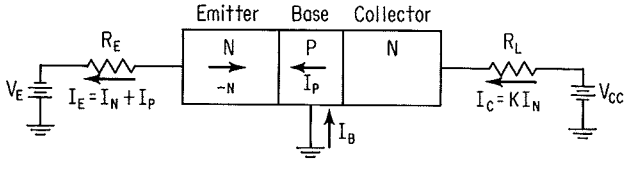

Fig. 1-1. Grounded-base connection of grown-junction transistor.

arithmetic sum of I_N and I_P.* Electrons injected into the P-type base region migrate (diffuse) toward the collector-base junction. Certain of these electrons combine with holes in the base region and no longer exist; those electrons which do not recombine in the base cross over into the collector region. A positive electric field, caused by V_{CC}, exists in the collector material, and electrons entering the collector from the base are quickly swept through the collector region to the external circuit.

For the present analysis, the assumption is made that no multiplication of electrons occurs in the collector region and that collector external current is determined solely by the electron current, which, after leaving the emitter region, is able to traverse the base layer and reach the collector region. A collector-base reverse-leakage current is also neglected in this discussion. The load resistor R_L is considered to be sufficiently small to have no effect upon collector-current magnitude.

Collector current I_C is shown in Fig. 1-1 to equal KI_N, where K is the ratio between electrons flowing out of the collector into the external circuit and the number of electrons which were injected into the base by the emitter. Because multiplication of electrons in the collector region is assumed not to exist at present, K is necessarily less than 1. Later, an analysis of factors affecting K will include the collector-region multiplication effect.

A forward current gain α_N is defined for the common-base configuration as the ratio of collector current to emitter current and is written†

$$\alpha_N = \frac{I_C}{I_E} \tag{1-1}$$

From the preceding discussion,

$$I_C = KI_N \tag{1-2}$$

and

$$I_E = I_N + I_P \tag{1-3}$$

Substitution of Eqs. (1-2) and (1-3) into Eq. (1-1) gives

$$\alpha_N = \frac{KI_N}{I_N + I_P} = \frac{K}{1 + I_P/I_N} \tag{1-4}$$

Equation (1-4) shows that even if there were no loss of electrons in the base region ($K = 1$), α_N would still be less than unity.

The preceding discussion of electron and hole injection into the base and emitter regions, respectively, gave no restrictions as to the relative magnitudes of these two carrier flows. Proper fabrication of the emitter and base regions can cause many more electrons to be injected into the base than there are holes injected into the emitter, and I_N becomes much larger than I_P. External emitter current is then

* Conventional current flow is in the opposite direction to electron flow.

† This gain is a forward gain in that the transistor is operated in the normal configuration with the emitter terminal and collector terminal of the device connected in the circuit so that they are biased as emitter and collector, respectively. The symbol α_N is usually read "alpha normal" or "normal alpha." A subscript is attached to the basic symbol α for grounded-base current gain in order to distinguish this gain from an inverted common-base current gain to be described in a later section of this chapter.

composed almost entirely of electron flow, and, from Eq. (1-4), α_N approaches K.

The relative magnitudes of electron and hole injection across a P-N junction are determined by resistivity of the respective P- and N-type regions. A low-resistivity region has a large number of majority carriers as compared to a high-resistivity region. In a forward-biased diode fabricated from regions of different resistivity the lower-resistivity material injects more carriers across the junction than the high-resistivity material does.[4] If emitter resistivity of the transistor in Fig. 1-1 is much lower than that of the base, current flow across the base-emitter junction is principally electron flow.

For operating temperatures at which thermal generation of electron-hole pairs is relatively small (below 350° C), resistivity of a semiconductor material is determined primarily by the number of P- or N-type impurities present in the material.[5] Intrinsic semiconductor material is doped with P- and N-type impurities in order to give transistor action. A highly doped region is one which has a large number of impurities and consequently a low resistivity. Proper doping of emitter and base regions gives typical emitter and base resistivities of 0.01 and 1.0 ohm-cm, respectively.[6]

The ratio of injected current from the emitter to the total external emitter current is referred to as the emitter injection efficiency and has the symbol γ_S.[7,*] This injection efficiency can be written

$$\gamma_S = \frac{I_N}{I_N + I_P} \tag{1-5}$$

A comparison of this expression with Eq. (1-4) shows that current gain α_N is proportional to γ_S. Equation (1-4) can be rewritten

$$\alpha_N = \gamma_S K \tag{1-6}$$

Thus far in the analysis of transistor current gain, only the effect of emitter injection efficiency has been considered in detail. The other factor affecting current gain is given in Eqs. (1-4) and (1-6) as the term K, which is the ratio between carriers entering the collector external circuit and the number of carriers leaving the emitter and entering the base region. For the N-P-N transistor shown in Fig. 1-1, electrons enter the base from the emitter. A certain number of these electrons recombine in the base and are thus unable to flow into the collector. The number of electrons flowing into the collector depends upon the average lifetime of electrons in the base region and the transit time of electrons through this region. If the base width is made small, so that the minority carriers injected into the base diffuse through this region in a shorter time than the average lifetime of these carriers in the base region, only a small number of recombinations will occur. The average lifetime of carriers injected into the base is dependent upon the number of available majority carriers (holes in the N-P-N transistor) in the base region. A high base resistivity thus allows more injected carriers to pass through to the collector. A narrow base width is essential to reduce transit time of these injected carriers and to increase the number of carriers which reach the collector.

* The subscript S is used here to denote a static, or large-signal, value of γ (gamma) as opposed to the small-signal parameter described in Ref. 7.

The ratio between the number of carriers which flow from the base into the collector and the number of carriers entering the base from the emitter is termed the "base transport factor" and is represented by β_S.* This term is different from K, as β_S is a function of carriers entering the collector, whereas K is a function of carriers leaving the collector and flowing into the external circuit. If the number of carriers entering the collector is not equal to the number leaving the collector, K and β_S are not equal.

The factor K is the product of two terms and is written

$$K = \beta_S M \tag{1-7}$$

where M is a collector-current multiplication factor.

In the N-P-N transistor, electrons which flow from base to collector are accelerated by the positive collector supply voltage to a fairly high velocity. If this velocity is sufficiently large, those electrons which happen to strike semiconductor atoms will release other electrons; these freed electrons flow toward the positive voltage source and may, in turn, release still other electrons. When this condition occurs, many more electrons leave the collector than the total number of those injected by the emitter into the base.

Collector-current multiplication is dependent upon the transistor structure and also upon the collector supply voltage. At low values of collector voltage, M is only slightly greater than unity. As collector voltage increases, this collector-current mutiplication factor becomes larger and may become almost infinite. The discussion of transistor breakdown voltage in Sec. 1-10 examines this breakdown effect more closely.

If the expression for K in Eq. (1-7) is substituted into Eq. (1-6), the current-gain expression becomes

$$\alpha_N = \gamma_S \beta_S M \tag{1-8}$$

This equation shows that the common-base current gain can be related to three separate factors. The device designer strives to adjust doping level, base width, and transistor geometry to give a $\gamma_S \beta_S$ product close to unity. Also, multiplication of carriers must be small at reasonable values of collector voltage. Thus far, only the α_N characteristic of a transistor has been considered. Requirements on other parameters of the device may make it necessary to compromise somewhat on one or more of the terms on the right side of Eq. (1-8).

1-3. INVERTED OPERATION

The transistor shown in Fig. 1-1 is composed of a P-type region of semiconductor material between two N-type regions. One N region of the device is designated as an emitter, and the other N region is specified as a collector. The discussion in Sec. 1-2 has shown how, for the N-P-N structure, a forward-biased emitter-base junction causes electrons to flow from the emitter, through the base, and into the collector region. A reverse bias on the collector-base diode causes emitter-injected electrons to flow through the collector material and into the external collector

* The subscript S designates a large-signal value for the base transport factor.

circuit. If the emitter and collector terminals of this transistor are interchanged, transistor action will still occur, with the collector material emitting electrons and the emitter region collecting those electrons which pass through the base. A current gain is defined for this inverted connection as

$$\alpha_I = \frac{I_E}{I_C} \tag{1-9}$$

where α_I is the inverted current gain of the transistor.

Although collector and emitter regions of a transistor are fabricated from material of the same conductivity, i.e., either N-type or P-type material, the two regions do not usually have the same resistivity or the same geometry. Emitter and collector regions are required to perform different functions, and each is usually designed to serve as emitter or collector, but not as both. For this reason, an inverted connection of most transistors does not give so large a current gain as the forward connection does; there is still transistor action, however, and α_I is not zero.

1-4. COMMON-BASE COLLECTOR CHARACTERISTICS

Figure 1-2 shows a plot of collector-current versus collector-base voltage for various values of emitter current. For values of collector-base voltage equal to or greater than zero volts and below the collector breakdown voltage, collector current is given by

$$I_C = \alpha_N I_E + I_{CBO} \tag{1-10}$$

where I_{CBO} is the collector-base diode reverse-leakage current.* This expression shows that for I_E equal to zero, collector current exists and is a leakage current. The $I_E = 0$ curve in Fig. 1-2 shows this operating condition. For reverse bias on the base-emitter junction, a slight reverse emitter current flows, and Eq. (1-10) is still valid. Thus collector current can be made less than I_{CBO} by reverse biasing the base-emitter junction. The region of transistor operation for which both the collector-base and emitter-base junctions are reverse-biased is defined as region I and is shown in the figure. This region is often referred to as one of collector-current cutoff.

A second region of transistor operation is shown in the figure as region II. In this region, the collector-base junction is reverse-biased, and the emitter-base

* This leakage current is often designated I_{CO}.

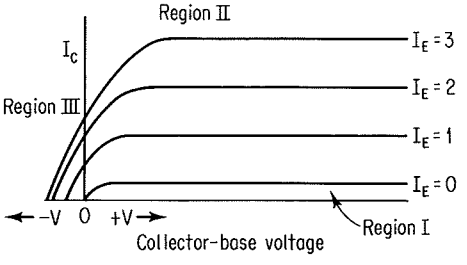

Fig. 1-2. Common-base collector characteristics.

junction is forward-biased. This is the region of transistor operation which is most often considered in a study of transistor operating principles.

Region III is shown in the figure to include that portion of the collector characteristic curves which lies to the left of the vertical axis. In this operating region, the emitter-base diode is forward-biased, as in region II, but the collector-base diode is no longer reverse-biased. As transistor operation moves to the left in region III, the collector-base voltage becomes sufficiently negative to forward-bias the collector-base diode. When this occurs, a saturation effect appears in the transistor. The saturated mode of operation is an important consideration in the design of many transistor switching circuits and is discussed further in the following secton.

1-5. COLLECTOR-CURRENT SATURATION

In the grounded-base transistor circuit of Fig. 1-3*a*, collector current causes a voltage drop V_R across the collector load resistor R_L, and the collector voltage is less positive than the collector supply voltage V_{CC}. As long as the collector voltage is above ground potential, the collector is positive with respect to the base, and emitter-injected electrons which enter the collector region flow into the collector external circuit. Figure 1-3*b* shows a plot of minority-carrier (electron) density in the base region for this condition. The points E and C along the horizontal axis show locations of the emitter and collector junctions, respectively.* This density plot shows that there is an electron gradient in the base region, with the electron density being greatest at the emitter junction and zero at the collector junction. This gradient is understandable, as the greatest concentration of electrons in the base occurs at the emitter junction, where electrons are injected into the base; there are no electrons present at the collector junction, because the collector removes all electrons which reach this junction.

Collector voltage in the above discussion can be made less positive by an increase in applied base-emitter voltage. This increased voltage causes a larger emitter current to flow, and consequently collector current is increased. The voltage drop across R_L becomes larger, and the collector voltage decreases toward ground potential. As the base-emitter voltage is further increased, an operating condition is reached at which the voltage drop V_R is equal to the magnitude of V_{CC}.

* Depletion layers existing at the two P-N junctions are not relevant to the present discussion and are neglected; they are described in Secs. 1-10 and 2-2.

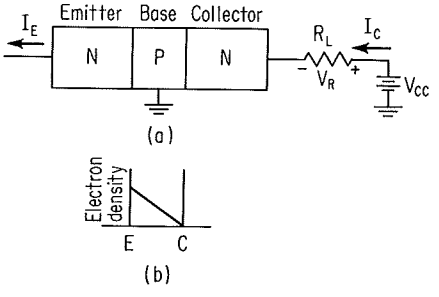

Fig. 1-3. *(a)* **Nonstandard transistor;** *(b)* **minority-carrier density in base region.**

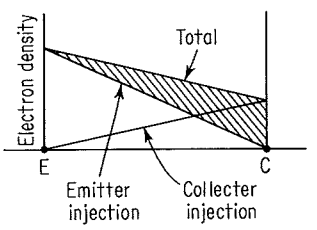

Fig. 1-4. Minority-carrier density in base of saturated transistor.

The collector and base are then at the same potential, and transistor operation enters region III.

A further increase of base-emitter voltage causes V_R to become even larger, and the collector-base junction becomes forward-biased. The collector serves as an emitter and injects electrons into the base, while at the same time it accepts a sufficient number of emitter-injected electrons to maintain the I_C value. Figure 1-4 shows electron-density gradient in the base region for this operating condition.[8] Collector-injected electrons cause a change in the gradient, as shown; the crosshatched area shows the excess of electrons in the base. The collector is unable to maintain a zero electron concentration at its junction with the base, and the transistor is considered to be in saturation.

An increase of forward-bias voltage on the emitter-base diode has caused the transistor to become saturated. If this voltage is reduced, the emitter does not inject so many electrons into the base, and electron concentration in the base becomes lower. However, as long as this concentration is not zero at the collector junction, the transistor remains in saturation. As emitter current continues to be lowered, the collector can more readily accept the reduced number of emitter-injected electrons and can also accept a larger portion of those electrons which it injects into the base; concentration of electrons in the base now approaches zero at the collector junction. When the collector-base diode is no longer forward-biased, because of a reduction of emitter current, the transistor comes out of saturation.

The time lapse between a reduction of emitter current and a reduction of collector current is important in many switching circuits where the transistor is allowed to saturate. A sudden decrease in emitter current does not immediately cause a corresponding decrease in collector current. This is because the excess carriers stored in the base cause collector current to remain approximately constant during the time interval required for the collector to reduce the charge concentration at the collector junction to zero.

The preceding analysis has shown that because the collector behaves as an emitter, there is a turnoff delay in a saturated transistor. This delay is often referred to as a "storage-time delay" because it is caused by excess charge stored in the base. In order to reduce storage-time effects, the collector should not perform well as an emitter. This can be accomplished by making the collector of high-resistivity material, thus causing collector injection efficiency to be low. A high collector resistivity is one reason why α_I of a transistor is usually lower than α_N. Ohmic resistance of the collector region places an upper limit on collector resistivity.

1-6. COMMON-EMITTER COLLECTOR CHARACTERISTICS

The relationship between emitter, collector, and base currents in a transistor is given by

$$I_E = I_C + I_B \tag{1-11}$$

where I_B is the base current. Substitution of the right side of this expression into Eq. (1-10) for I_E gives, after rearrangement of terms,

$$I_C = \frac{\alpha_N I_B}{1 - \alpha_N} + \frac{I_{CBO}}{1 - \alpha_N} \tag{1-12}$$

The coefficient of I_B in Eq. (1-12) can be written

$$\frac{\alpha_N}{1 - \alpha_N} = \frac{I_C/I_E}{1 - I_C/I_E} = \frac{I_C}{I_E - I_C} = \frac{I_C}{I_B} \tag{1-13}$$

Similarly, the coefficient of the I_{CBO} term can be rearranged to give

$$\frac{1}{1 - \alpha_N} = \frac{I_C}{I_B} + 1 \tag{1-14}$$

The term β_N introduced here is defined to be

$$\beta_N = \frac{I_C}{I_B} \tag{1-15}$$

Thus, β_N is a ratio of collector current to base current and is the forward current gain of a grounded-emitter transistor. This transistor connection, shown in Fig. 1-5, is also referred to as the "common-emitter configuration." Input current to the transistor is now considered to be I_B, whereas for the grounded-base configuration the current I_E was considered to be the input current. Forward current gain of the common-emitter connection is considerably larger than α_N of the same transistor.

From the above discussion, Eq. (1-12) can be rewritten

$$I_C = \beta_N I_B + \frac{I_{CBO}}{1 - \alpha_N} \tag{1-16}$$

$$I_C = \beta_N I_B + (\beta_N + 1) I_{CBO} \tag{1-17}$$

These expressions show that collector leakage current at zero input current is increased over what it was in the common-base configuration.

A plot of I_C versus collector-emitter voltage can be obtained for various values of I_B as shown in Fig. 1-6. These curves are the common-emitter collector characteristic curves and are important in the design of many types of transistor circuits. Switching-circuit design relies heavily upon information obtained from curves of this type. This information may be presented graphically, as by the curves, or it may be tabulated as measured dc parameters of the transistor. Certain of the dc parameters which can be obtained from these curves are discussed in Secs. 1-8 to 1-10.

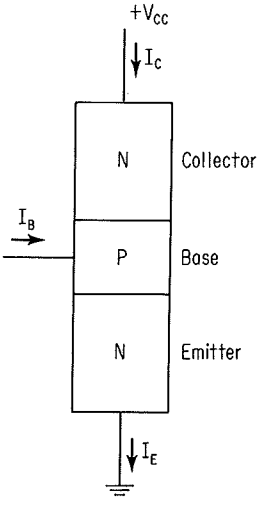

Fig. 1-5. Grounded-emitter transistor connection.

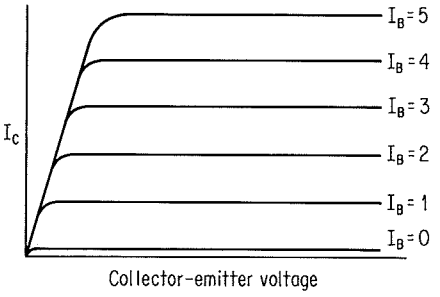

Fig. 1-6. Common-emitter collector characteristic curves.

1-7. BASE AND COLLECTOR POTENTIALS IN THE COMMON-EMITTER CONFIGURATION

When the transistor is designed into a switching circuit, dc current levels in the circuit are determined by external supply voltages, resistance values of the discrete components connected to the transistor, and voltage drops within the transistor itself. The grounded-emitter connection is often used for a transistor switching circuit; voltage levels of the base and collector terminals relative to ground potential are of concern. Because the emitter is at ground potential, the base and collector potentials are usually referred to as "base-emitter voltage" and "collector-emitter voltage," respectively. Base-emitter voltage has the symbol V_{BE}, and collector-emitter voltage has the symbol V_{CE}.

Input current to the common-emitter circuit is a base current into the base-emitter diode. If the collector is open-circuited, a plot of I_B versus V_{BE} is the typical current-voltage plot of a forward-biased diode, as shown in curve A of Fig. 1-7. If collector voltage is now applied and a small collector current is allowed to flow, the current-voltage plot for the input diode becomes that of curve B of the figure. As collector current increases still further, the input plot is that of curve C. These plots show that base-emitter voltage drop depends upon the value of collector current and increases for larger values of I_C.

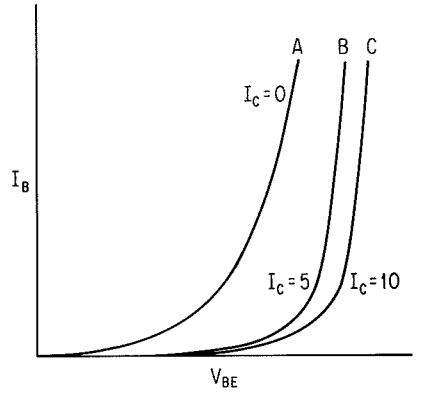

Fig. 1-7. Effect of collector current on base-emitter voltage.

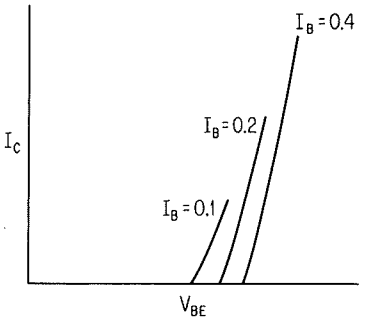

Fig. 1-8. Another method of displaying relationship between transistor currents and voltages.

A second method of displaying the relationship between I_B, V_{BE}, and I_C is illustrated by the plots of Fig. 1-8, which show that the magnitude of allowable collector current is dependent upon the value of base current. Of course, this is also shown by the collector characteristics of Fig. 1-6.

The value of V_{BE} for a low-power germanium switching transistor is nominally between 0.2 and 0.4 volt for moderate values of collector current and base drive. Silicon transistors have larger values of V_{BE}, typically between 0.6 and 0.8 volt.

A relationship between V_{CE}, I_C, and I_B is indicated in the collector characteristic curves of Fig. 1-6. These curves show that the voltage from collector to emitter is always of the same polarity. If collector ohmic resistance is neglected, the voltage from collector to emitter is

$$V_{CE} = V_{BE} + V_{CB} \tag{1-18}$$

When the transistor saturates, the voltage V_{CB} reverses polarity, although its magnitude is always less than that of V_{BE}. The collector-emitter voltage of a saturated transistor is the difference between two small voltages and is a small voltage. This saturation voltage is often written as $V_{CE(\text{sat})}$. Transistors are sometimes operated in the inverted connection to reduce the value of transistor saturation voltage.[9,10] The emitter is now the collector terminal and has a good injection efficiency when the transistor is saturated. This low value of saturation voltage is obtained at the expense of a reduced forward current gain for the circuit.

Ohmic resistance of the collector region causes the value of $V_{CE(\text{sat})}$ to be larger than that given by Eq. (1-18). An accurate expression for the saturation voltage drop is

$$V_{CE(\text{sat})} = V_{BE} + V_{CB} + I_C R_{CS} \tag{1-19}$$

where R_{CS} is the ohmic resistance of the collector, including any contact resistance at the junction of the collector material and the external lead.

The effect of collector-emitter voltage in switching-circuit design is considered in Chap. 4. It is shown that a low value of $V_{CE(\text{sat})}$ is desirable in many types of switching circuits. For this reason, a low value of collector ohmic resistance is usually desired in a transistor switch.

Values of $V_{CE(\text{sat})}$ for certain types of germanium and silicon low-power switching transistors may be as low as 0.1 volt for collector currents as large as 50 ma.

1-8. LEAKAGE CURRENTS

For reverse voltages well below the diode breakdown voltage, a small current flows through a reverse-biased P-N junction. Referred to as "diode leakage current," it has two components. The first of these components is a true diode reverse current, given by[4,*]

$$I = I_s(e^{qV/KT} - 1) \tag{1-20}$$

where I_s = diode saturation current
q = electronic charge

* Equation (1-20) is derived in Sec. 2-2.

V = applied diode voltage in volts
K = Boltzmann's constant
T = absolute temperature

For reverse-bias voltages greater than a few tenths of a volt, the magnitude of I is approximately equal to that of I_s. Diode saturation current is a function of the diode material and the temperature of the diode. At room temperature (25°C), I_s is usually less than 0.1 μa for a silicon diode and less than 1.0 μa for a germanium diode. For both diode types, the magnitude of I_s doubles with approximately each 10°C increase in diode temperature.

The second component of diode leakage current is a surface leakage component, which is not temperature-dependent but which increases as the reverse voltage is increased. This current flows through whatever shunt resistance exists between the diode terminals. Careful surface treatment of the diode can make this component of leakage current negligibly small.

Diode leakage current exists in a reverse-biased transistor. However, because there are now three regions of semiconductor material, as opposed to two regions for the diode, external current flow into or out of the device is often not of the same magnitude as that of the diode leakage current.

I_{CBO}. Consider the transistor configuration shown in Fig. 1-9*a*. The emitter terminal is open, and current flow into the collector terminal is the reverse leakage current of the collector-base diode; this current is given the symbol I_{CBO}. The first two subscripts indicate the two transistor terminals to which voltage is applied, and the third subscript indicates the electrical connection of the third terminal. In this case, the third terminal is the emitter terminal, and the subscript O shows that the emitter terminal is open. This reverse-current flow is often referred to as "collector cutoff current."

I_{CEO}. The transistor connection of Fig. 1-9*b* causes collector leakage current to become larger than I_{CBO}. The base terminal is now open-circuited, and external base current does not flow. From Eq. (1-16), for $I_B = 0$,

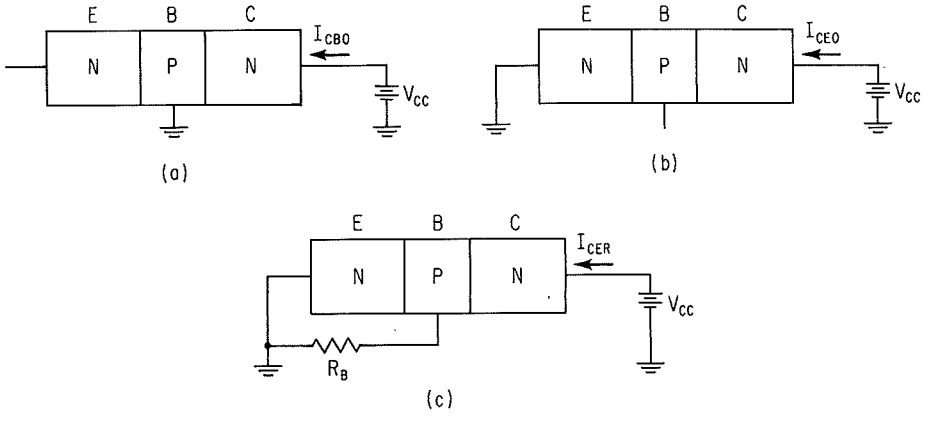

Fig. 1-9. Leakage currents for various transistor connections.

$$I_C = \frac{I_{CBO}}{1 - \alpha_N} \tag{1-21}$$

This expression shows that for α_N near unity, the magnitude of collector leakage current can be very large. Collector leakage current for this open-base condition is designated I_{CEO}.

I_{CER}, I_{CES}. In the circuit configuration of Fig. 1-9*b*, the base of the transistor is slightly positive with respect to the emitter. If a resistor is now connected from the base to emitter, as in Fig. 1-9*c*, a small current will flow out of the base into ground.[11] This current is in the opposite direction to normal base-current flow in an N-P-N transistor and is determined by the magnitude of base-emitter voltage and the value of resistor R_B. Equation (1-16) is still valid for this negative base current, and the value of collector current is reduced over the open-base connection.

A resistor as large as 20 kilohms will cause a considerable decrease in collector leakage current from the I_{CEO} level. As the external base resistor is reduced, more reverse base current flows, and the value of collector leakage current is further reduced. Collector leakage current for a given value of resistor is referred to as I_{CER}.

For a short circuit between the emitter and base terminals, collector leakage current is lower than for the resistive connection and has the symbol I_{CES}, where the subscript S indicates that the base and emitter terminals are shorted to each other. Ebers and Moll[2] have derived expressions for the collector leakage current with base shorted to collector, base connected to emitter through a resistor, and base open. For the shorted base connection in a junction transistor, collector leakage current is shown to be

$$I_{CES} = \frac{\alpha_I I_{CBO}}{1 - \alpha_N \alpha_I} \tag{1-22}$$

An expression for I_{CER} as a function of R is also presented, which, as R approaches infinity, gives the expression of Eq. (1-21).

I_{CEX}. In many switching-circuit designs, reverse voltages are applied to both the base and collector terminals, as shown in Fig. 1-10. The reverse-bias base-emitter voltage causes a small emitter current to flow out of the base terminal. This emitter current has a negative value and causes collector-current magnitude, given by Eq. (1-10), to become less than I_{CBO}. Collector current under this operating condition has the symbol I_{CEX} (the X indicates a reverse bias on the base).

The plots of Fig. 1-11 show typical values of collector leakage current for a germanium alloy-junction transistor under the following conditions:

1. Base-emitter junction reverse-biased ($V_{BE} = -0.1$ volt).
2. Base shorted to emitter ($R_B = 0$ ohms).
3. A resistor of 20 kilohms connected between base and emitter ($R_B =$ 20 kilohms).
4. Base terminal open ($R_B = \infty$ ohms).

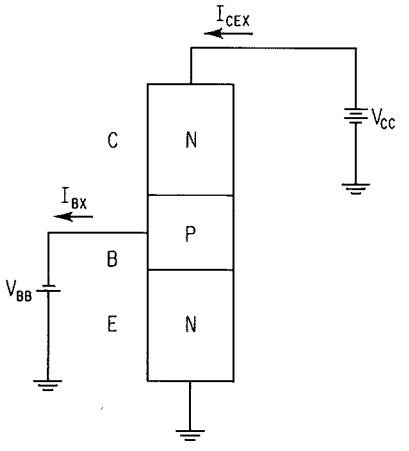

Fig. 1-10. Transistor connection for operation in region I.

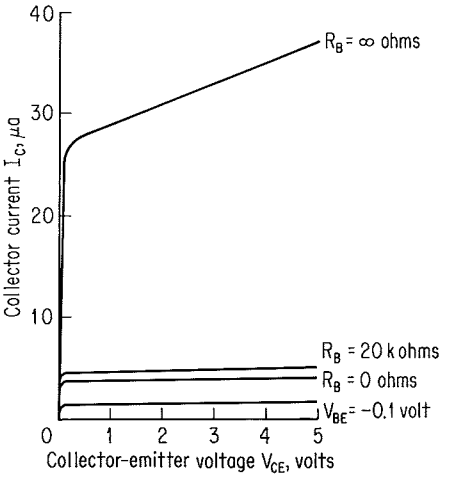

Fig. 1-11. Typical plots of various collector leakage currents for a germanium alloy-junction transistor.

These curves are a portion of the common-emitter collector characteristic curves discussed briefly in Sec. 1-6. Collector-emitter voltage in Fig. 1-11 is well below the collector breakdown voltage of the device. The vertical scale is expanded to show the differences in collector leakage currents.

I_{BX}. Base current in the circuit configuration of Fig. 1-10 is the sum of currents flowing from collector and emitter regions. This reverse base current is designated I_{BX}.

I_{EBO}. If a reverse-bias voltage is applied between emitter and base terminals, with the collector terminal open-circuited, a diode leakage current flows through the base-emitter diode. This current is an emitter cutoff current and has the symbol I_{EBO}.

Each of the leakage currents described above is measured at a specified value of applied voltage. Leakage currents increase as applied voltage is made larger.

1-9. COLLECTOR-CURRENT CUTOFF

The above discussion of leakage currents has shown that collector current can be reduced to a small value, even though the base-emitter diode is not reverse-biased. The transistor is at the edge of region I, the region of collector-current cutoff, for collector leakage current equal to I_{CBO}. Operation is in region I when base-emitter and collector-base junctions are simultaneously reverse-biased, and collector leakage current is equal to I_{CEX}. However, because the leakage currents described above as I_{CBO}, I_{CER}, and I_{CES} are of the same order of magnitude as region-I collector leakage current I_{CEX}, the transistor is considered to be at collector-current cutoff for collector current equal to I_{CBO}, I_{CER}, or I_{CES}. Leakage current I_{CEO} may be much larger than I_{CEX}, and the transistor cannot safely be considered to be at collector-current cutoff when the base terminal is open-circuited.

1-10. BREAKDOWN VOLTAGES

Figure 1-12 shows an N-P-N transistor with a reverse-bias voltage applied between the collector-base diode; the emitter terminal is open-circuited. Holes in the P-type base region are attracted toward the negative terminal of the battery, and electrons from the N-type collector region are attracted toward the positive terminal of the battery. The P-type material has a deficiency of holes in a small region close to the collector-base junction. Acceptor atoms in this region have been stripped of their positive charge by the externally applied voltage. Similarly, the external voltage has removed electrons from donor atoms close to the junction in the N-type collector material. Thus, a region exists at the collector-base junction which contains neither holes nor electrons.[12] This region is often referred to as a "depletion layer" or "space-charge region" and is shown in Fig. 1-12 to have the length *d*.

The collector-base current which flows under this reverse-bias condition is a diode leakage current. Most of the voltage drop in the above circuit occurs across the depletion layer, and an electric field exists across this region.

As the external voltage is increased, more holes and electrons are attracted toward the base and collector terminals, respectively, and the depletion layer extends farther into both regions of the collector-base diode. Penetration depth of the depletion layer into a semiconductor material depends upon resistivity of the material. The number of carriers removed in a depletion layer is determined by the applied voltage. Because a high-resistivity material has fewer carriers than a region of low resistivity, the depletion layer, for a fixed external voltage, extends farther into a high-resistivity region than into a region of low resistivity.

If the P and N regions of the collector-base diode have the same resistivity, the depletion layer penetrates into each region an equal amount. Unequal resistivities will cause the depletion layer to penetrate farther into one region than into the other. Resistivity of the base region is considerably higher than that of the collector region. The large base resistivity is necessary to give a good emitter injection efficiency, and the low collector resistivity reduces voltage drop across the collector material. Thus, the depletion layer extends farther into the base than into the collector. An increasing external collector-base voltage may cause the space-charge region to reach the emitter-base junction. The electric field now extends completely across the base region, and punch-through has occurred.[13]

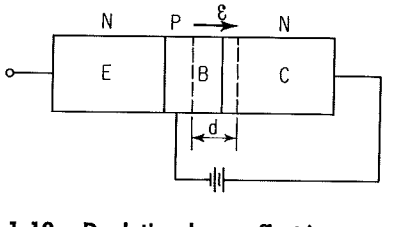

Fig. 1-12. Depletion-layer effect in reverse-biased collector-base diode.

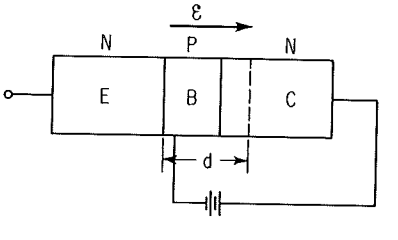

Fig. 1-13. Punch-through caused by the depletion layer's extending across the entire base region.

Figure 1-13 shows the punch-through condition. If an external circuit is now connected to the emitter terminal of the transistor in Fig. 1-13, current flow between the emitter and collector terminals is limited only by resistivity of the two N regions and by external resistance.

A second type of transistor breakdown occurs because of the electric field which exists across the depletion layer at the collector-base junction. Carriers entering this electric field are accelerated to a high velocity. Certain of these carriers collide with bound electrons and generate electron-hole pairs. These freed carriers may, in turn, acquire sufficient velocity to generate additional holes and electrons.[14] This effect is often termed "avalanche multiplication." Avalanche breakdown of a transistor is caused by multiplication of carriers in the collector-base depletion layer and may also be caused by multiplication in the collector material itself. Because collector resistivity is not zero, an electric field exists in the collector material; this field can cause avalanche multiplication.

The curve of Fig. 1-14 shows the avalanche breakdown which occurs across the collector-base diode of a germanium-alloy transistor. The emitter terminal is open-circuited for this measurement. The figure shows that, for large values of applied voltage, collector current rises toward infinity. The effect of avalanche breakdown is to multiply the original collector current by the factor[15]

$$M = \frac{1}{1 - (V/V_B)^n} \tag{1-23}$$

where M = collector-current multiplication factor
V = applied voltage
V_B = applied voltage at which M becomes infinite
n = constant between approximately 3 and 6

The term M is the same as that presented in Eq. (1-7).

Voltage punch-through in a transistor causes a short circuit in the device, and transistor action no longer occurs. Avalanche multiplication, however, does not inhibit transistor action.[16] Equation (1-23) shows that avalanche multiplication occurs for even small values of applied (collector) voltage. As this voltage approaches V_B, the multiplication factor becomes infinitely large.

Two sets of letter symbols are presently used to designate transistor breakdown voltages. The earlier nomenclature consists of the letters BV, followed by three subscripts. These subscripts are interpreted in the same manner as explained previously for leakage-current nomenclature. The newer letter symbols, published

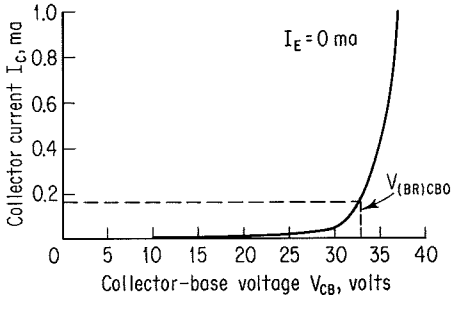

Fig. 1-14. Collector-base breakdown curve for germanium-alloy transistor.

Table 1-1. Definitions of Commonly Used Breakdown-voltage Designations

Breakdown voltage	Terminals measured across	State of third terminal
$V_{(BR)CBO}$, BV_{CBO}	Collector-base	Emitter open-circuited
$V_{(BR)CEO}$, BV_{CEO}	Collector-emitter	Base open-circuited
$V_{(BR)CES}$, BV_{CES}	Collector-emitter	Base shorted to emitter
$V_{(BR)CER}$, BV_{CER}	Collector-emitter	Base connected to emitter through a resistor
$V_{(BR)CEV}$, BV_{CEX}	Collector-emitter	Base-emitter junction biased with a voltage source (BV_{CEX} indicates a reverse-bias voltage only)
$V_{(BR)EBO}$, BV_{EBO}	Base-emitter	Collector open-circuited

in IEEE Standard 255, December, 1963, consist of the symbol $V_{(BR)}$ followed by three subscripts, which are interpreted as before, except that a forward or reverse bias to the base is now designated by a V instead of an X. Several of the commonly used breakdown-voltage designations are listed in Table 1-1. The newer breakdown symbols are given first; these symbols are used in further references to breakdown voltages.

Transistor leakage currents are specified for particular values of collector-base, collector-emitter, or base-emitter voltage. Transistor breakdown voltages are specified at particular values of transistor leakage currents. For instance, the voltage $V_{(BR)CBO}$ may be measured at a collector current of 10 μa. When the emitter terminal is open-circuited, collector-base voltage of the transistor is increased until collector leakage current is equal to 10 μa. The $V_{(BR)CBO}$ rating of the transistor is equal to the magnitude of applied collector-base voltage which gives the 10-μa current level. The plot of Fig. 1-14 shows the effect of collector-base voltage upon collector leakage current and indicates one current level at which $V_{(BR)CBO}$ can be specified.

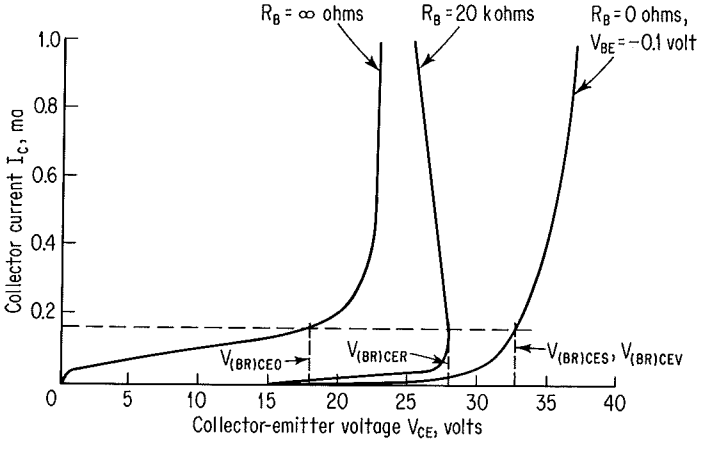

Fig. 1-15. Collector-emitter breakdown curves for germanium-alloy transistor: R_B is external resistance from base to emitter.

A transistor has the largest collector breakdown voltage when connected in the common-base configuration. The value of $V_{(BR)CBO}$ is larger than any of the collector breakdown voltages associated with the common-emitter configuration. In many transistor types, the $V_{(BR)CBO}$, $V_{(BR)CES}$, and $V_{(BR)CEV}$ breakdown voltages are nearly identical. Figure 1-15 shows typical collector-breakdown curves for the grounded-emitter connection of a germanium-alloy transistor. (The same transistor was used to determine Figs. 1-14 and 1-15.) A comparison of Figs. 1-14 and 1-15 shows that there is no noticable difference between the $V_{(BR)CBO}$, $V_{(BR)CES}$, and $V_{(BR)CEV}$ curves.

Figure 1-15 shows that at low current levels, the $V_{(BR)CEV}$ (or $V_{(BR)CES}$) and $V_{(BR)CEO}$ ratings are the maximum and minimum collector-emitter breakdown voltages, respectively. At higher current levels, the breakdown curve for $R_B =$ 20 kilohms is asymptotic to the curve for $R_B = \infty$ ohms.

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2

Small-signal Equivalent Circuit of Junction Transistor

2-1. INTRODUCTION

Transistor characteristic curves showing dc properties of the junction device were presented in Chap. 1. These large-signal plots are useful with respect to choosing a transistor having adequate dc characteristics and also for selecting suitable steady-state operating conditions of current and voltage. Certain aspects of ac operation can be derived from these graphical presentations of transistor characteristics.

As an example of the manner in which ac parameters can be determined from plots of dc characteristics, consider the common-emitter collector characteristic curves shown in Fig. 2-1. A tangent is drawn at point A on a curve of constant base current. The slope of this line is the ratio $\Delta_1 I_C/\Delta V_{CE}$. As the increment ΔV_{CE} approaches zero, the above ratio becomes the common-emitter hybrid parameter h_{oe}, and is written

$$h_{oe} = \lim_{\Delta V_{CE} \to 0} \frac{\Delta_1 I_C}{\Delta V_{CE}} = \frac{i_c}{v_{ce}} \tag{2-1}$$

where i_c = incremental change in collector current
v_{ce} = incremental change in collector-emitter voltage
The common-emitter hybrid parameter h_{fe} can also be derived from the figure.

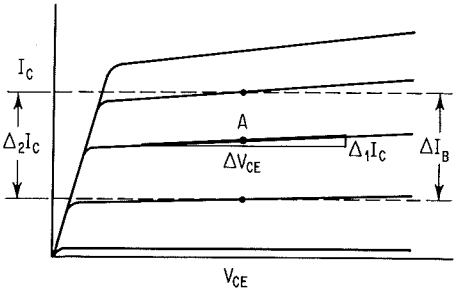

Fig. 2-1. Graphical construction to determine h_{oe} and h_{fe}.

This parameter exists at point A when ΔI_B approaches zero and is written

$$h_{fe} = \lim_{\Delta I_B \to 0} \frac{\Delta_2 I_C}{\Delta I_B} = \frac{i_c}{i_b} \tag{2-2}$$

where i_b is the incremental change in base current.

Two additional hybrid parameters can be obtained from the V_{BE} versus V_{CE} plots of Fig. 2-2. The common-emitter hybrid parameters h_{re} and h_{ie} are determined at point B and are written

$$h_{re} = \lim_{\Delta V_{CE} \to 0} \frac{\Delta_1 V_{BE}}{\Delta V_{CE}} = \frac{v_{be}}{v_{ce}} \tag{2-3}$$

where v_{be} is the incremental change in base-emitter voltage, and

$$h_{ie} = \lim_{\Delta I_B \to 0} \frac{\Delta_2 V_{BE}}{\Delta I_B} = \frac{v_{be}}{i_b} \tag{2-4}$$

The hybrid parameters discussed above are defined in terms of a four-terminal representation of the transistor.[1] Figure 2-3 shows this network representation, together with the input variables i_b and v_{be} and the output variables i_c and v_{ce}. A relationship among these variables can be described by

$$v_{be} = h_{ie} i_b + h_{re} v_{ce} \tag{2-5}$$

$$i_c = h_{fe} i_b + h_{oe} v_{ce} \tag{2-6}$$

All terms in the above two equations are ac quantities. The hybrid parameters can be determined graphically as described above, or they can be measured with small ac signals applied to the transistor. Equations (2-5) and (2-6) are represented by the ac equivalent circuit of Fig. 2-4; Eq. (2-5) is a voltage equation for the left-hand loop of the equivalent circuit, and Eq. (2-6) is a current equation for the right-hand loop of the circuit. This ac equivalent circuit is useful to calculate low-frequency transistor performance at the bias conditions for which the hybrid parameters were measured. However, the nature of these ac parameters is such that they merely characterize the transistor as a "black box" and do not enable a

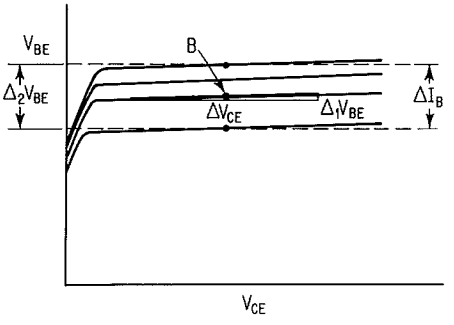

Fig. 2-2. Graphical construction to determine h_{re} and h_{ie}.

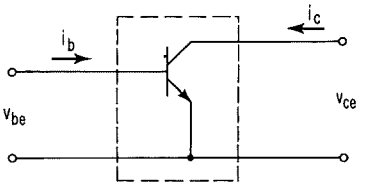

Fig. 2-3. Transistor as a four-terminal network.

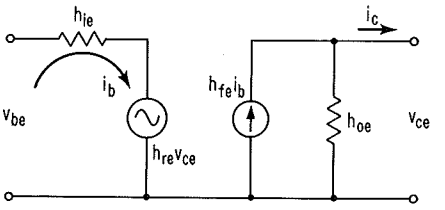

Fig. 2-4. Hybrid equivalent circuit of transistor.

designer to predict performance accurately over a wide frequency range or over an extensive variation of current and voltage levels.

Many ac, or small-signal, equivalent circuits have been developed for the transistor.[2] Among these are circuits which relate various transistor parameters to physical operation of the semiconductor device. One advantage of this latter type of small-signal equivalent circuit is that transistor performance can be associated with the particular technique used for fabrication of the device. This enables the circuit designer to choose a transistor more intelligently from among the many different types manufactured by a variety of methods. Because equivalent-circuit parameters are now related to the physics of the semiconductor device, the effects of circuit changes involving current, voltage, and frequency levels can be evaluated. Also, this equivalent-circuit representation provides the device engineer and circuit designer with a common model which they can use to discuss possible changes in transistor parameters.

Small-signal equivalent circuits which show a relationship between elements of the equivalent circuit and physical operation of the transistor may range from complex to relatively simple models. Although the more complex equivalent circuits generally give accurate results, they are often difficult to use in a mathematical analysis. Conversely, while a relatively simple equivalent circuit can be readily analyzed, the extreme simplicity of the circuit may lead to inaccurate results.

One small-signal equivalent circuit which relates device parameters to physical operation of the transistor is described in the following section. This circuit, which is a good compromise among the many more complex and simpler circuits which have been derived, is valid for region II of transistor operation. Although numerical values of the circuit parameters are constant for only small excursions about a dc operating point, the effects of wide variations in operating current and voltage levels can be determined. Frequency response of the transistor is also included in the equivalent-circuit representation. This circuit is used in Chap. 4 to evaluate transient response of a transistor switch.

2-2. COMMON-BASE SMALL-SIGNAL EQUIVALENT CIRCUIT

Figure 2-5 shows a small-signal equivalent circuit for the common-base connection of a grown-junction transistor. The grown-junction device is selected for discussion because of the relative simplicity of its equivalent circuit. Modifications to this circuit can be made for the newer transistor types. The given circuit resembles an early T low-frequency equivalent circuit of a transistor, although more elements are now included.[3] Inclusion of capacitors, together with a

frequency-dependent collector-current generator, permits accurate circuit analysis over a broader frequency range than could be obtained with the simple T circuit. Unlike the elements of the T circuit, the various components of the present equivalent circuit are directly related to transistor physical operation.

In order to derive elements of the above equivalent circuit, it is first necessary to describe charge-carrier flow in a semiconductor material in somewhat more detail than presented in Chap. 1. The first principle considered is the concept of diffusion. An electron or a hole contributed by an impurity atom in a semiconductor crystal is free to move throughout an N- or P-type region, respectively. For the present analysis, electron motion is described; the same kinetic principles also apply to holes. Consider an N-type crystal to which no external voltage is applied. The distribution of free electrons is assumed uniform throughout the crystal. Concentration of free electrons is regarded as sufficiently small so that these electrons do not affect each other by their presence. Thus, there are no electric fields acting upon a free electron. Thermal energy of these electrons gives them a random motion, and they wander about within the crystal. This type of motion is referred to as "diffusion." Individual electrons initially grouped into a cluster at one spot within the crystal tend to diffuse throughout the crystal and spread away from each other.[4]

Consider now an initial concentration of free electrons which varies from left to right in the crystal, as shown in Fig. 2-6. Electron density is greatest at x equal to zero and decreases linearly with increase in x. A concentration gradient exists and is equal to the rate of change of charge density with respect to distance. This gradient is simply the slope of the line shown in the figure. As time increases from the instant at which the charge density has the gradient shown, random motion of the electrons causes the charge distribution to change. Eventually, there will be a uniform distribution of mobile electrons throughout the crystal. Since there are initially more charges on the left side of the crystal, a net charge flow to the right must occur in order to establish the uniform charge distribution. This electron flow causes a net current flow to the left within the crystal. An important principle of transistor operation is that *charges flow from regions of high concentration to regions of low concentration.*

A second important aspect of carrier flow in a semiconductor element is the principle of charge flow across a P-N junction. Figure 2-7*a* shows a P-N junction

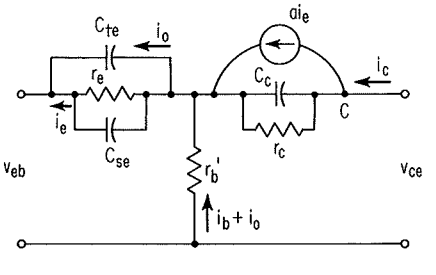

Fig. 2-5. Common-base small-signal equivalent circuit.

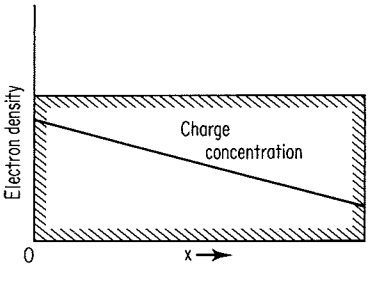

Fig. 2-6. Crystal with nonuniform charge distribution.

diode which contains an N-type region and a P-type region. The entire diode is one continuous semiconductor crystal fabricated of either germanium or silicon. If there were no forces exerted on free carriers in the two regions, carrier concentration in the diode would simply vary from an excess of one type of impurity to an excess of the other type. There would then be a location within the diode at which there were neither holes nor electrons. This infinitesimally small region of charge neutrality would exist at the physical junction of the P and N regions. However, it will be seen that there is a finite region between the P and N portions of the diode which contains neither free holes nor free electrons.

With no external bias applied to the diode of Fig. 2-7*a*, some electrons on the left side of the junction diffuse into the P region, and some holes on the right side of the junction diffuse into the N region. The electrons and holes, which are majority carriers in the N and P regions, respectively, become minority carriers in the opposite-polarity regions into which they diffuse. Those minority carriers which cross the junction diffuse a short distance away from the junction before they recombine with free carriers of opposite polarity. The average distance which a minority carrier traverses before it recombines is referred to as the "diffusion length" of the carrier.

Electrons and holes near the junction are seen to diffuse across the junction. The diffusion of these charges causes electrostatic forces to be set up, which prevent additional free carriers of one region from diffusing across the junction into the other region.[5] This can be understood by analyzing charge flow across the junction. Donor atoms, which contribute excess electrons in the N region, are fixed in place within the crystal structure. As electrons near the junction diffuse into the P region, donor atoms in the vicinity of the junction are stripped of their mobile charges. These donor atoms, which were originally electrically neutral, are now left with a net positive charge. Acceptor atoms contribute mobile holes in the P region. A number of these holes diffuse across the junction, and acceptor atoms near the junction are left with a net negative charge. Diffusion of electrons and holes across the junction thus creates an electric field, which retards additional flow of these mobile charges.

A small region containing no mobile charges extends on either side of the physical junction and is the depletion layer, or space-charge region, described in Sec. 1-10. This depletion layer, which is caused by diffusion of electrons and holes away from the N and P regions, respectively, creates a potential barrier to additional diffusion of majority carriers out of a region. The potential barrier retards the flow of majority carriers across the junction, but it does not prohibit this flow entirely. Figure 2-7*a* illustrates the depletion layer at the diode junction, and Fig. 2-7*b* shows the potential difference existing across

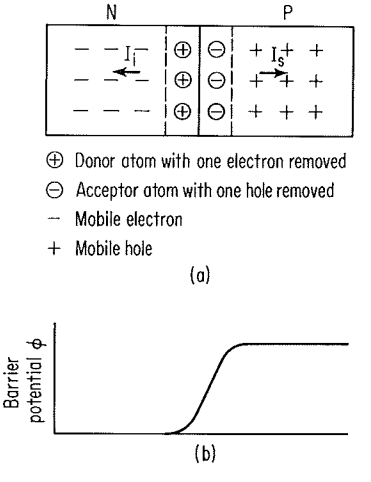

Fig. 2-7. *(a)* **Charge distribution in P-N junction diode;** *(b)* **potential barrier across depletion layer.**

the depletion layer. In this discussion, electrons are considered to run downhill normally and holes are considered to run uphill normally. Thus, the potential diagram represents a barrier to the flow of both electrons and holes.

A certain number of electrons and holes succeed in overcoming the potential barrier. These carriers give rise to a forward component of diode current, termed an "injection current." The number of carriers flowing against the potential barrier is dependent upon the thermal energy of the carriers and the height of the barrier. Statistical mechanics shows that there is an exponential relationship between height of the barrier and the number of carriers which overcome the barrier. Injected current I_i is proportional to carrier flow against the barrier and is written[4]

$$I_i = K_0 e^{q\phi/KT} \tag{2-7}$$

where K_0 = constant
q = electronic charge
ϕ = barrier potential
K = Boltzmann's constant
T = absolute temperature

If a short-circuit path is connected across the two ends of the diode, an external current cannot flow, as there are no active elements in the circuit. Yet, solely on the basis of the preceding analysis, it would appear that the current I_i would flow through the external conducting path. A reverse component of internal diode current exists which exactly cancels the current I_i. This reverse current is caused by thermal generation of electrons and holes in the two regions. Consider the process occurring in the P region. Thermal energy within the crystal enables an electron to break away from an acceptor atom. Generation of a free electron in this manner causes a hole to appear where the electron existed; thermal generation of carriers thus produces pairs of electrons and holes. An electron freed in the above fashion is strongly influenced, by the electric field existing between itself and its paired hole, to become again part of the acceptor atom's electronic structure. Although many of the freed electrons do fall back into the vacancy which they created, a number of them diffuse about within the P region. Those electrons which do reach the potential barrier shown in Fig. 2-7*b* encounter a potential hill, which they readily slide down and thus cross the junction. A similar process occurs in the N region for generated holes. The reverse component of current resulting from thermally generated minority carriers crossing the junction is termed a "saturation current" and is given the symbol I_s. This current is independent of the height of the potential hill.

Currents I_i and I_s are shown in Fig. 2-7*a* and are seen to flow in opposite directions to each other. Net current flow I through the diode is the difference between these two currents and is written

$$I = I_i - I_s \tag{2-8}$$

An applied voltage of either polarity across the diode terminals modifies the potential barrier and causes an increase or a decrease in injected current. Ohmic resistance of the diode is small, and voltage drop within the diode is considered to appear entirely across the depletion layer. Thus, the potential hill is equal in

magnitude to voltage across the diode terminals. Replacement of ϕ with applied diode voltage V in Eq. (2-7) and substitution of the right side of this expression for I_i in Eq. (2-8) yield

$$I = K_0 e^{qV/KT} - I_s \tag{2-9}$$

The constant K_0 is readily evaluated by making use of the knowledge that I_i and I_s are numerically equal for a short circuit across the diode ($V = 0$). If V is set equal to zero in Eq. (2-9), K_0 is determined to be $-I_s$. The expression for diode current is now written

$$I = I_s(e^{qV/KT} - 1) \tag{2-10}$$

r_e. The above equation, which relates dc current through a P-N junction to voltage across the junction, is valid for the base-emitter diode of a transistor. An ac conductance is derived from this expression by considering the effect of small changes in applied diode voltage. This is accomplished by differentiating the equation with respect to V to obtain

$$\frac{dI}{dV} = g_e = \frac{q}{KT} I_s e^{qV/KT} \tag{2-11}$$

where g_e is the ac conductance of the emitter-base diode. Consider now the exponential multiplier in Eq. (2-10). For a forward diode voltage much greater than KT/q, the term qV/KT becomes very large. As the magnitude of KT/q is approximately 0.026 at room temperature (+25°C), a small forward voltage of 10×0.026, or 0.26 volt, is large enough to make the -1 term of the equation insignificantly small. Thus, for usual values of forward base-emitter voltage, the diode current can be expressed

$$I = I_s e^{qV/KT} \tag{2-12}$$

The left side of this expression can be substituted into Eq. (2-11) to yield

$$g_e = \frac{q}{KT} I \tag{2-13}$$

which gives

$$r_e = \frac{1}{g_e} = \frac{KT}{qI} \tag{2-14}$$

where r_e is the ac resistance of the emitter-base diode. Replacement of I in Eq. (2-14) with emitter current I_E and substitution of the room-temperature value for KT/q into this same expression give

$$r_e = \frac{26}{I_E} \tag{2-15}$$

where r_e is in ohms and I_E is the dc emitter current in milliamperes. Because the derivation of Eqs. (2-12) to (2-15) neglects the -1 term of Eq. (2-10), the effect of I_s is not considered in Eq. (2-15). This latter expression is very nearly correct for emitter currents equal to or greater than 10 times the value of I_s. At room

temperature, Eq. (2-15) is valid for emitter currents greater than approximately 30 μa for most germanium transistors and greater than approximately 5 μa for most silicon transistors.

C_{se}. Minority-carrier density in the base region was described in Sec. 1-5. The greatest concentration of electrons in the base of an N-P-N transistor was found to exist at the emitter junction, with the density varying linearly to zero (for a nonsaturated transistor) at the collector junction. Figure 2-8 shows a transistor biased for operation in region II, together with three plots of minority-carrier density within the base region. Base width W is seen to be less than it would be if a space-charge region did not exist at the emitter and collector junctions. Curve A shows the gradient existing for a nominal value of emitter current I_E. If base-emitter voltage is made more positive, additional carriers are injected into the base region, and the carrier distribution becomes that of curve B. This charge distribution causes the new value of emitter current I_E' to be larger than I_E. Similarly, a reduction of base-emitter voltage gives a charge distribution within the base as shown in curve C; emitter current I_E'' is now less than I_E.

An ac voltage applied to the input of a transistor causes a continuous redistribution of base charge, as described above. This redistribution of charge, which is necessary to increase or decrease emitter current, is identical to the process of supplying more or less charge to a capacitor.[5] Emitter-storage capacitance C_{se} is included in the small-signal equivalent circuit to represent the above process. This capacitance is also referred to as "emitter-diffusion capacitance."

C_{te}. The depletion layer existing at a P-N junction was seen to be caused by removal of mobile charges in the P and N regions. An electric field exists across this space-charge region and prevents additional holes or electrons from crossing over into the opposite-polarity region. An applied voltage across the junction causes the electric field to increase or decrease and respectively widens or narrows the depletion layer. This flow of charge for variation of junction voltage is a capacitive effect; the space-charge region is considered to be a capacitor having two parallel plates separated by the width of the region.[6] A capacitance of this nature is referred to as a "transition capacitance." The transition capacitance existing across the emitter-base junction is shown in the equivalent circuit of Fig. 2-5 as C_{te}, the emitter-transition capacitance.

r_b'. Base-current flow in a transistor requires that base resistance r_b' be included in the small-signal equivalent circuit. One component of base current is a result

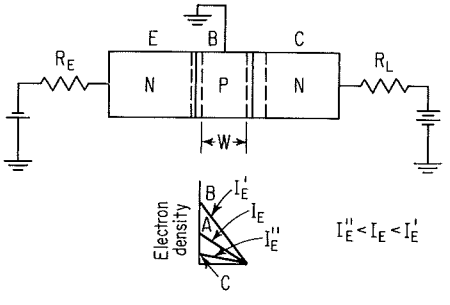

Fig. 2-8. Transistor biased for linear operation and base-region charge-density plots.

of the less-than-unity injection efficiency of the forward-biased emitter-base diode. As holes are injected into the emitter of an N-P-N transistor, holes are created by electron flow out of the base terminal to maintain a constant hole concentration in the base. Because the base transport factor is also less than unity, a second component of base current is established by recombination, in the base, of majority carriers with emitter-injected minority carriers. For the N-P-N transistor, new holes are created at the base terminal to compensate for those holes which are lost by recombination. Both components of base current require that electrons leave the base terminal of an N-P-N transistor. Thus, a current flow into the base is established for this type of transistor.

Figure 2-9 represents a grown-junction transistor and shows several paths of current flow within the base. This current flows to the various points of carrier recombination and also flows to the edge of the emitter-base depletion layer. The width of the base region is narrow compared to its height, so that the above base-current flow is nearly parallel to the plane of the emitter-base junction. This current is at right angles to the diffusion current across the transistor and is a *transverse* base current. Transverse base current flowing through ohmic resistance of the base region gives a voltage drop between the base terminal and the emitter-base junction of the transistor. This ohmic resistance is represented in the equivalent circuit by r_b'. Transverse base current actually comes from a point source (the base contact) and spreads out somewhat within the base region. For this reason, the resistance r_b' is often referred to as a "base-spreading resistance."[7]

a. A current generator is included in the small-signal equivalent circuit of Fig. 2-5. Input current to the equivalent circuit consists of the total current flowing through r_e, C_{se}, and C_{te}. Currents through r_e and C_{se} contribute to the presence of minority charges in the base region. Current flow into C_{te} (the current i_o) serves only to modify the total charge of the depletion-layer capacitance and does not affect minority-carrier density in the base region. Because collector current is due to minority carriers of the base region diffusing across into the collector region, it is clear that only the components of current through r_e and C_{se} contribute to collector current. The internal-current generator, depicted by the product of i_e and device parameter a, shows the relationship between i_e and total ac current available at the collector region of the transistor.

For junction transistors, the capacitance C_{te} is considerably smaller than C_{se}, and the total input current to the transistor is usually considered to be the current i_e. The current generator is an ac circuit element and amplifies emitter current of either polarity. Thus, in the circuit of Fig. 2-5, current ai_e flows either into or out of point C. Parameter a is considered to be the internal small-signal current gain of the transistor.

The discussion of Sec. 1-2 pointed out that the large-signal transistor parameter α_N is the product of large-signal values of emitter injec-

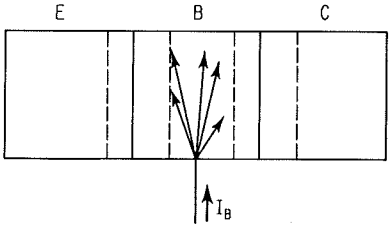

Fig. 2-9. Paths of base-current flow within the transistor.

tion efficiency, base transport factor, and collector-current multiplication factor. Transistor parameter a is the product of the small-signal values of the above three factors and is expressed

$$a = \gamma\beta m \tag{2-16}$$

where γ = small-signal value of emitter injection efficiency
β = small-signal value of base transport factor
m = small-signal value of collector-current multiplication factor*

The nature of a is described by first considering its small-signal low-frequency characteristic and then its behavior at higher frequencies. Total behavior of a is then expressed as the product of a dc term modified by a frequency-dependent term.

A small-signal low-frequency value for a is determined for infinitesimally small dc variations of collector and emitter current about a fixed operating point. Let the terms γ_o, β_o, and m_o represent small-signal low-frequency values of γ, β, and m, respectively. From Eq. (2-16),

$$a = \gamma_o\beta_o m_o g(\gamma,\beta,m) \tag{2-17}$$

where $g(\gamma,\beta,m)$ is a frequency-dependent function of γ, β, and m. The parameter a_o is defined to be

$$a_o = \gamma_o\beta_o m_o \tag{2-18}$$

Substitution of a_o into Eq. (2-17) yields

$$a = a_o g(\gamma,\beta,m) \tag{2-19}$$

The term a_o is the small-signal low-frequency value of a. Common-base forward current gain α_N, defined by Eq. (1-1), is the large-signal low-frequency equivalent of a_o. Magnitudes of α_N and a_o are identical only if there is equal spacing between the emitter-current steps of Fig. 1-2. However, the two parameters have approximately equal magnitudes.

The frequency-dependent term $g(\gamma,\beta,m)$ of Eq. (2-19) is analyzed by consideration of frequency variations of γ, β, and m. There is some frequency variation of γ, but its effect upon current gain is considerably less than the effect caused by frequency variation of β.[8,9] The parameter m is not significantly affected by frequency, and Eq. (2-19) can be reduced to

$$a = a_o g(\beta) \tag{2-20}$$

Diffusion paths of slightly different lengths exist for the various carriers which pass from the emitter, through the base region, to the collector junction. In addition, average velocity of a minority carrier through the base region may be slightly different from that of other identical carriers which traverse this region. The above two effects of diffusion give rise to a spread in transit time, or "dispersion," of minority carriers through the base region.[10] As input-signal frequency is increased, dispersion causes a decrease in collector-current magnitude, and β decreases.[11,12]

* The terms γ, β, and m are small-signal values of the factors γ_S, β_S, and M described in Sec. 1-2.

For a low-level input signal of ω radians/sec at the emitter of an N-P-N common-base stage, the term β can be expressed[13]

$$\beta = \operatorname{sech}(1 + j\omega\tau_n)^{1/2}\frac{W}{L_n} \tag{2-21}$$

where τ_n = lifetime of electrons in base region
W = width of base region
L_n = diffusion length of electrons in base region

The terms τ_n, W, and L_n are determined by the structure and impurity concentration of the transistor; these terms are considered to have constant values for the small variation of input signal. Calculated values of amplitude and phase shift, for various values of ω, are obtained from the above expression and plotted in Fig. 2-10. At low frequencies, the amplitude plot has the magnitude a_o. The amplitude and phase curves completely describe device parameter a, as both the dc and ac characteristics of small-signal current gain are displayed.

Amplitude of a is displayed in Fig. 2-10 as a decibel plot. The value of a_o is considered to be unity, and has a magnitude of 0 db at low frequency. As ω increases in value, the magnitude of a begins to decrease; the radian frequency at which a has decreased to -3 db is defined as ω_a. At radian frequencies beyond ω_a, the amplitude curve falls at a constant 6 db/octave.

An approximate expression for a is[14]

$$a = \frac{a_o}{1 + j\omega/\omega_a} \tag{2-22}$$

This expression, which is of the form used to describe an RC type of cutoff, gives

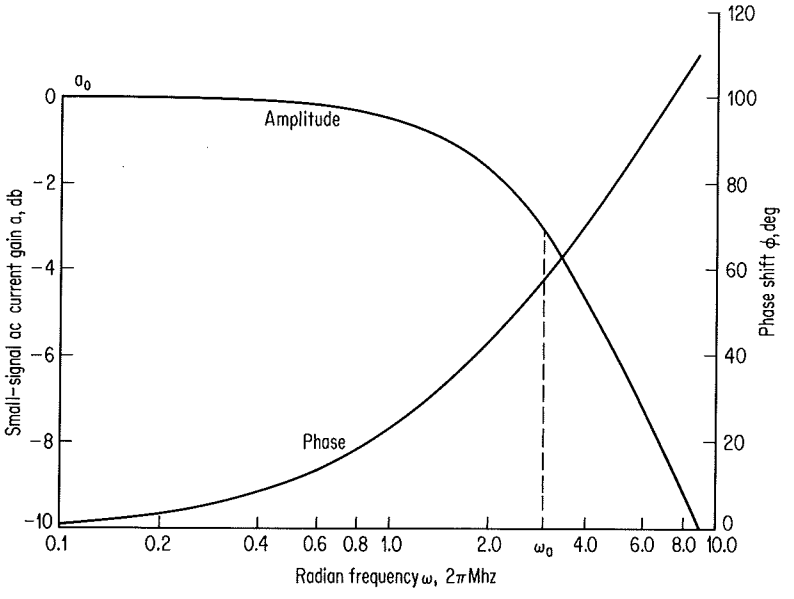

Fig. 2-10. Theoretical amplitude and phase plots of a versus radian frequency.

a phase shift at ω_a of 45°. The phase plot of Fig. 2-10 shows that the actual phase shift at ω_a, as determined from Eq. (2-21), is 57°. Thus although the amplitude of a varies as the frequency response of an RC network, the phase shift of a at the -3-db point is 12° larger than that experienced by the RC circuit; this added phase lag is termed "excess phase."

A more exact expression to describe amplitude and phase of a is[2,15,16]

$$a = \frac{a_o e^{-jm\omega/\omega_a}}{1 + j\omega/\omega_a} \tag{2-23}$$

where m is excess phase at ω_a and is equal to 0.2 radian for the transistor under discussion. The above equation gives the same amplitude plot as Eq. (2-22), but phase shift is now closer to that obtained from Eq. (2-21). Figure 2-11 shows plots of amplitude and phase shift as determined from Eqs. (2-21) to (2-23). The abscissa of this figure is shown as ω/ω_a. Equation (2-23) is seen to give a close approximation to the theoretical-amplitude and phase-shift plots determined from Eq. (2-21).

Equation (2-22), though it gives a less exact representation of a than Eq. (2-23), is relatively easy to manipulate and is to be used in Chap. 4 for transient calculations.

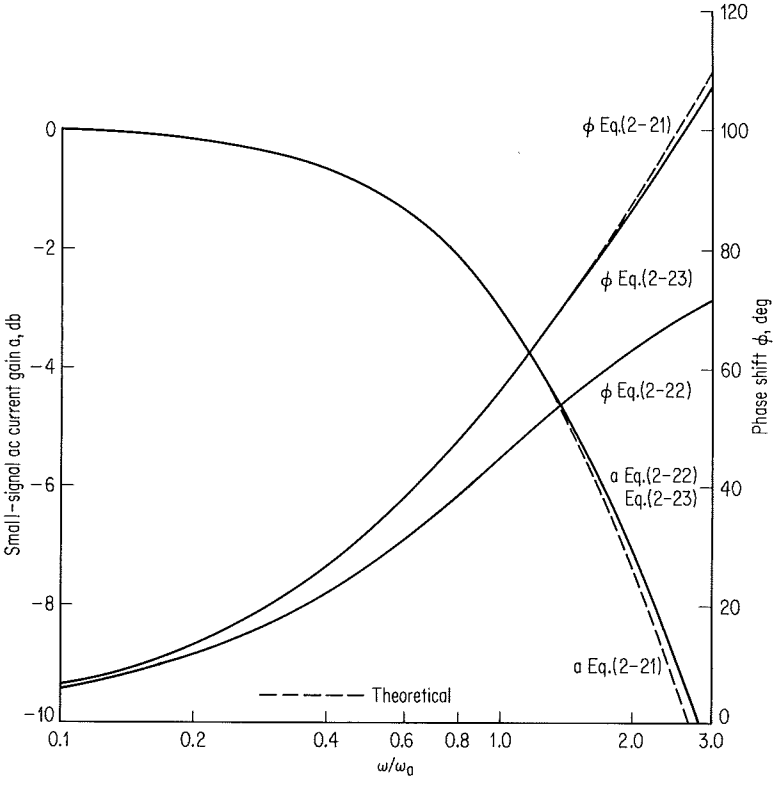

Fig. 2-11. Amplitude and phase plots of a versus normalized radian frequency from theoretical and approximate equations.

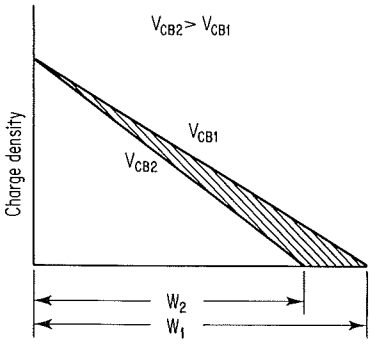

Fig. 2-12. Minority-carrier concentration gradient in base region for two levels of collector-base voltage.

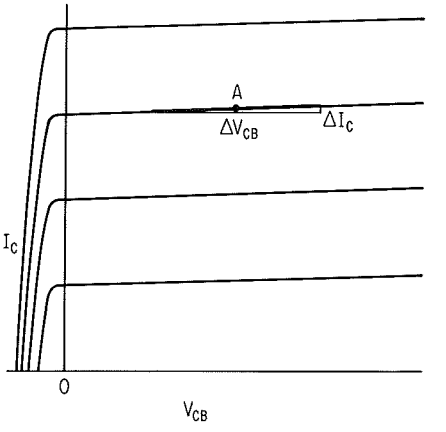

Fig. 2-13. Graphical construction to determine r_c.

Radian frequency ω is divided by 2π to give frequency f. The frequency f_a, corresponding to ω_a, is the common-base cutoff frequency of the transistor. Parameter a is considered to be ac alpha (common-base current gain) of the transistor, and cutoff frequency f_a is often referred to as the "alpha cutoff frequency" of the transistor.

C_c. Two capacitance effects are present in the collector portion of the transistor. Collector-base reverse bias causes a depletion-layer capacitance at the collector junction; this capacitance is designated C_{tc}. The second capacitance effect is caused by the voltage-dependent nature of the above depletion layer. As v_{cb} is made larger, this depletion layer extends farther into both the collector and base regions. Width of the base region decreases, and a new minority-carrier concentration must be established in the base region.[16] Emitter injection remains constant, and minority-carrier concentration at the base edge of the depletion layer must continue to be zero (as the transistor is not in saturation). Figure 2-12 shows minority-carrier density in the base region for two values of applied collector-base voltage. As voltage is increased from V_{CB1} to V_{CB2}, the base width decreases from W_1 to W_2. An excess of base charge, shown as the shaded portion of the figure, must now be removed. The necessary redistribution of base charge, caused by variation of base width, gives an equivalent collector-storage capacitance C_{sc}. However, this storage capacitance is usually negligibly small compared to C_{tc} and is neglected in the present equivalent circuit.[7] Total collector capacitance is given as C_c in the equivalent circuit of Fig. 2-5 and represents depletion-layer capacitance of the collector-base junction.

r_c. Collector ac resistance r_c is the ratio of an incremental change in collector-base voltage to the resultant incremental change in collector current for a fixed value of emitter current. This resistance is described with the aid of the common-base collector characteristic curves shown in Fig. 2-13. A tangent is drawn at point A, and the differential quantities ΔI_C and ΔV_{CB} are shown. Collector

resistance is defined as

$$r_c = \lim_{\Delta I_C \to 0} \frac{\Delta V_{CB}}{\Delta I_C} = \frac{v_{cb}}{i_c} \tag{2-24}$$

where v_{cb} = incremental change in collector-base voltage
i_c = incremental change in collector current

If the plots of constant emitter current in Fig. 2-13 were parallel to the horizontal axis, the slope at point A would be zero, and collector ac resistance would be infinite. The curves show, however, that even after the transistor comes out of saturation, there is a slight increase in I_C for a large increase in V_{CB}. The tangent drawn at point A has a small slope; r_c is equal to the reciprocal of this slope and is usually in the order of megohms.

Collector resistance is analyzed by studying the influence of collector-base voltage on collector current. Two transistor effects cause r_c to be less than infinite. Variation of collector-base potential causes base width to vary as described previously in the discussion of collector-storage capacitance. Figure 2-12 shows that the concentration gradient of minority carriers in the base region changes as the base width varies. Minority-carrier flow across the base region is proportional to the existing concentration gradient and consequently changes as collector-base voltage varies. Collector current, which is determined principally by the above minority-carrier flow, thus varies with change in collector-base voltage. An increase in v_{cb} narrows the base width, minority-carrier concentration increases, and i_c increases.

The second transistor effect which influences r_c is collector-current multiplication. As v_{cb} increases in magnitude, avalanche multiplication increases and i_c becomes larger. Avalanche multiplication and depletion-layer widening both cause i_c to increase as v_{cb} is made larger; these two occurrences give a finite positive value of r_c.

2-3. EFFECT OF DC OPERATING POINT UPON PARAMETERS OF EQUIVALENT CIRCUIT

Small-signal equivalent-circuit parameters of the transistor are dependent upon dc current and voltage levels. This dependence is often an important factor in the selection of quiescent operating points for both saturated and nonsaturated switching circuits. In addition, selection of total current and voltage excursions is often based upon a qualitative knowledge of the above parameter variations.

Two physical characteristics of the transistor are influenced by operating voltage and current levels: the first of these characteristics is width of depletion layers within the transistor, and the second is relative magnitudes of minority carriers and majority carriers in the base region. Certain of the small-signal parameters described previously can be related to these two physical characteristics and hence to dc operating levels.

Width of the depletion layer at a P-N junction was shown in Sec. 1-10 to be a function of the voltage applied across the junction. The transistor base region is physically located between the emitter-base and collector-base depletion layers;

width of this base region is dependent upon penetration of the two depletion layers into the base material. Base width is thus seen to be dependent upon voltage levels applied to the transistor.

Small defects in the base material, as well as the presence of base-region majority carriers, cause a certain number of minority carriers to recombine in the base region. Surface recombination of minority carriers also occurs in the base region. At extremely low levels of emitter current, the above two effects allow the number of minority carriers which reach the collector region to be only a small percentage of those carriers injected into the base by the emitter. As emitter current rises, more minority carriers are injected into the base, and a larger portion of these injected carriers is able to reach the collector junction.

In previous discussions of minority-carrier flow through the base region, it was implicit that the minority-carrier density was sufficiently small to have a negligible effect upon the electric field in the base region. At relatively large values of emitter current, however, this assumption is not valid. As minority-carrier density in the base region becomes comparable to the density of majority carriers, emitter current is no longer accurately expressed by Eq. (2-10). Also, an electric field is set up in the base region, which influences the flow of minority carriers toward the collector junction. In addition, base-region recombination of minority carriers is affected by the large density of these carriers.

Variation of r_e. The discussion of Sec. 2-2 pointed out that because of the manner in which Eq. (2-15) was derived, this expression is valid (at +25°C) only for emitter currents greater than approximately 30 μa for most germanium transistors and greater than approximately 5 μa for most silicon transistors. Another consideration regarding the low-current value of r_e is carrier generation in the base-emitter depletion layer.[17] For room-temperature operation at a relatively low value of applied forward voltage, this generated current may be considerably larger than I_s of a silicon transistor; the magnitude of I_s for a germanium transistor is sufficiently large for the effect of barrier-generated current to be neglected. The 5-μa level of emitter current in a silicon transistor is large compared to the above generated current and, for the silicon device, is a safe lower limit of current at which Eq. (2-15) may be applied.

Equation (2-15) shows that r_e is an inverse function of I_E. As I_E becomes larger, r_e decreases in direct proportion to the increase in current. However, this linear dependence of r_e upon I_E does not continue indefinitely. An increase of I_E results in a greater concentration of minority carriers in the base region. As this minority-carrier density becomes comparable to the density of majority carriers in the base region, majority carriers move to the base-emitter junction to neutralize the minority carriers. The rate of increase of injected carriers now becomes approximately $e^{qV/2KT}$ instead of $e^{qV/KT}$, as described in Sec. 2-2.[18] This smaller rate of increase for I_E causes emitter ac resistance to become larger than the value obtained from Eq. (2-15). The coefficient given in Eq. (2-14) as KT/q may now vary between approximately $1.5KT/q$ and $3KT/q$.[17]

Bulk resistance of the transistor, as well as series and contact resistance of the leads and bonds which connect the physical emitter to the outside of the transistor package, causes a high-current deviation of emitter ac resistance from that given

by Eq. (2-15). Values of r_e calculated from the above equation are usually valid for emitter currents as large as 10 to 200 ma, depending upon the type of transistor. The 10-ma current level is the probable upper limit of accuracy for calculations involving small-signal transistors having rated collector currents of approximately 200 ma. The 200-ma emitter-current level is associated with high-power transistors which are rated for collector currents greater than 1 amp.

Variation of C_{se}. The following expression has been derived for emitter-storage capacitance in terms of emitter ac conductance g_e and a cutoff frequency ω_1[19]

$$C_{se} = \frac{g_e}{1.5\omega_1} \tag{2-25}$$

The cutoff-frequency term is defined to be

$$\omega_1 = \frac{2D_p}{W^2} \tag{2-26}$$

where D_p = diffusion constant for holes
W = base width

Substitution of Eqs. (2-13) and (2-26) into Eq. (2-25) and replacement of I with I_E yield

$$C_{se} = \frac{qI_E W^2}{3.0KTD_p} \tag{2-27}$$

At moderate levels of emitter current, C_{se} increases in a linear fashion as the magnitude of I_E is made larger. At high levels of emitter current, the D_p term in Eq. (2-27) becomes dominant, as described below.

Minority-carrier flow through the base region results in a concentration gradient across the base. In order for charge neutrality to exist within the base region, there must also be a concentration gradient of majority carriers across the base. At low levels of emitter current, the gradient of majority carriers is not significant, but at high levels of emitter current, this gradient is of importance. Consider an N-P-N transistor operated at a level of emitter current sufficiently high to cause the number of injected electrons in the base region to be nearly as large as the original concentration of holes in this region. A hole-density gradient exists and causes a diffusion flow of holes in the same direction as the electron flow. However, as holes cannot flow into the reverse-biased collector region, an electric field is created, which causes a drift current of holes to flow in the opposite direction to the hole-diffusion current; these two components of hole current exactly cancel each other.[17] Electron flow is aided by the electric field, and electrons cross the base partly by diffusion and partly by drift. There is a resulting increase in electron current flow, and the diffusion constant D_p is effectively doubled.[20] As emitter current increases from a low level to a high level, C_{se} increases and then decreases. The magnitude of C_{se} at large emitter currents is approximately one-half the value determined by I_E acting alone.

Collector-base reverse voltage affects base width and, from Eq. (2-27), influences the value of C_{se}. An increase of applied voltage results in a decrease of W, and C_{se} becomes smaller. Width of the collector-base depletion layer varies

directly as the one-third power of voltage for a grown-junction device.[7] The resulting nonlinear relationship between applied voltage and base width causes a relatively small variation of C_{se} for a wide variation of V_{CB}.

Variation of C_{te}. Width of the emitter-base depletion layer has the same voltage dependency as described above for the collector-base depletion region. Emitter depletion-layer capacitance is at a maximum when the emitter-base junction is forward-biased and decreases as reverse-bias voltage is applied.

The magnitude of C_{te} is not dependent upon the level of dc emitter current.

Variation of a. Small-signal current gain a of the transistor is influenced by operating levels of dc voltage and current, In order to simplify the analysis of current- and voltage-level effects, dc operating voltage of the collector-base junction will be considered as being sufficiently small for collector-current multiplication effects to be negligible.

Consider first the manner in which the level of dc emitter current influences a. With reference to the terms on the right side of Eq. (2-17), the term m_o is equal to unity, the term γ is not affected by I_E, and the term m is neglected. Parameter a as a function of I_E can be written

$$a = \gamma_o h_1(I_E)\beta_o h_2(I_E) g(\beta) h_3(I_E) \tag{2-28}$$

where $h_1(I_E)$, $h_2(I_E)$, and $h_3(I_E)$ are functions of I_E. The first two terms of the above expression can be combined to give

$$a = a_o h_4(I_E) g(\beta) h_3(I_E) \tag{2-29}$$

where $h_4(I_E)$ is a function of I_E.

The term a_o in the above expression is a small-signal parameter whose magnitude is related to large-signal current gain α_N of the transistor; this is illustrated in Fig. 2-14, which shows collector characteristic curves of a transistor connected in the common-base configuration. For the particular device, α_N increases from 0.5 at operating point A to 0.9 at operating point B. If the transistor operates at point A, an assumed 0.4-ma change in emitter current gives the incremental

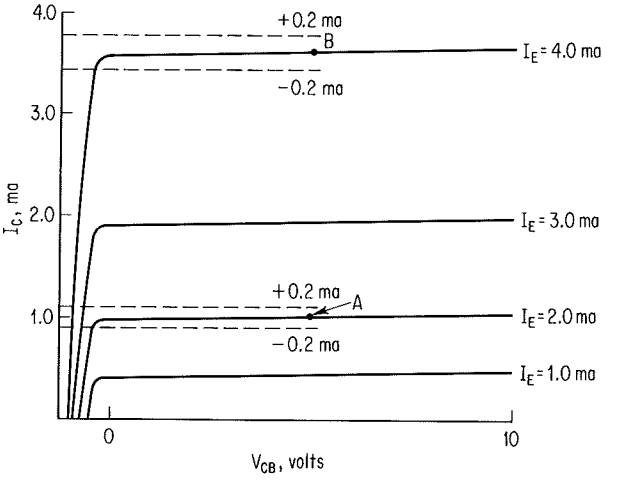

Fig. 2-14. Relationship between α_N and a_0.

collector-current change shown, while operation at point B gives a larger incremental collector current for the same 0.4-ma variation of emitter current. The small-signal value of current gain is larger at point B than at point A because the curves of constant emitter current are spaced farther apart in the vicinity of point B than they are in the neighborhood of point A. Because of the proportionality which exists between a_o and α_N, a can be written

$$a = K_1\alpha_N h_4(I_E)g(\beta)h_3(I_E) \tag{2-30}$$

where K_1 is a constant.

Collector-current multiplication effects are now neglected, and large-signal current gain can be written

$$\alpha_N = \gamma_S\beta_S \tag{2-31}$$

Substitution of the above expression into Eq. (2-30) gives

$$a = K_1\gamma_S h_5(I_E)\beta_S h_6(I_E)g(\beta)h_3(I_E) \tag{2-32}$$

where $h_5(I_E)$ and $h_6(I_E)$ are functions of I_E. Amplitude of parameter a changes because of modification of γ_S and β_S by I_E. Frequency variation of a is caused by the effect of I_E upon $g(\beta)$.

Rather than present analytic expressions for the functions $h_5(I_E)$, $h_6(I_E)$, and $h_3(I_E)$ of Eq. (2-32), the discussion will describe the manner in which the terms γ_S, β_S, and $g(\beta)$ vary with I_E. The composite variations of γ_S and β_S determine amplitude variation of a; these two large-signal terms are first considered.

Emitter injection efficiency was shown in Sec. 1-2 to be dependent upon relative magnitudes of electron and hole injection across an emitter-base junction. The ratio of carriers injected into the base to those injected into the emitter was seen to be proportional to the ratio of base resistivity to emitter resistivity. In order for γ_S to be close to unity, a transistor is fabricated to have an emitter resistivity which is considerably smaller than the base resistivity. However, at high levels of emitter current, there is in the base region a gradient of majority carriers in the same direction and of the same magnitude as the gradient of injected carriers. The large concentration of majority carriers causes a decrease in base resistivity, and a larger number of carriers are injected from the base into the emitter. This large increase in carrier flow into the emitter causes γ_S to decrease at high levels of I_E.[20]

Base transport factor is a measure of the number of emitter-injected carriers which succeed in passing through the base region to the collector region. A certain number of carriers which enter the base region recombine with opposite-polarity carriers before reaching the collector junction. Two types of recombination, surface recombination and volume recombination, determine β_S of the transistor.[20,21]

Large-signal current gain is determined by γ_S, surface recombination, and volume recombination. At low values of I_E, surface recombination is the predominant factor affecting α_N. As I_E increases somewhat, the resulting electric field within the base causes velocity of the minority carriers to increase, and surface recombination decreases. There is an initial increase in current gain as I_E in-

creases. At still larger magnitudes of I_E, both surface recombination and volume recombination decrease slightly to give a larger value of β_S.[22] However, the γ_S term is now the dominant factor affecting α_N; the resulting large decrease in γ_S causes α_N to decrease at higher levels of I_E.

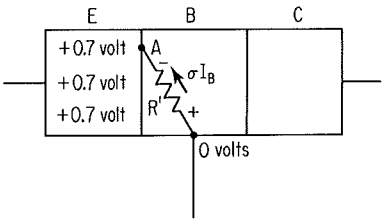

Fig. 2-15. Pinch-off effect occurs at high current levels.

At high levels of I_E, transverse base current reduces forward bias over a portion of the emitter edge, and there is nonuniform injection of carriers along the length of the emitter-base junction.[23,24] This is explained by reference to Fig. 2-15, which shows a filament of base current σI_B flowing from the base contact to point A in the base region; depletion layers at the emitter and collector junctions are neglected for simplicity. Ohmic resistance between the base contact and point A is represented by R'. Consider that the transistor is a silicon device and that potential at the base contact is taken as a reference. For a forward bias across the emitter-base junction, the emitter edge is an equipotential surface and has a positive voltage level of 0.7 volt. For the present analysis, assume that σI_B causes a voltage drop of 0.1 volt along R'. There is only 0.6 volt across the emitter-base diode at point A, and the junction is only slightly forward-biased. Forward bias is increasingly larger along the incremental emitter edges closer to the base contact. Very little carrier injection is obtained from the emitter surface above point A. The effective cross-sectional area of the emitter-base junction is reduced, and minority-carrier concentration in the base region is larger than if the above pinch-off effect did not occur. This effect causes a further reduction in γ_S, and α_N decreases even more at high levels of I_E.

Figure 2-16 shows a typical plot of α_N versus I_E for a grown-junction transistor. Surface recombination determines α_N at the current level I_E', and emitter injection efficiency determines α_N at the current level I_E''.

Frequency response of the $g(\beta)$ term of Eq. (2-32) increases as I_E is made larger.[21] The high velocity imparted to minority carriers (as a result of the electric field within the base region) causes a reduction in carrier transit time between emitter and collector junctions. This reduction in transit time has the effect of increasing the operating frequency range of the transistor. A high level of I_E extends frequency response of $g(\beta)$ but reduces the amplitude of a_o.

The effect of collector-base voltage on parameter a is now considered. At larger values of applied voltage, the resulting decrease in base width causes both amplitude and frequency response of the base transport factor to increase. Surface recombination and

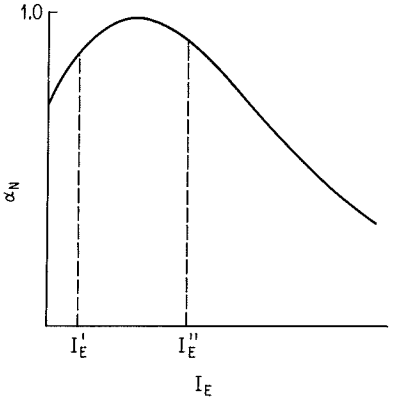

Fig. 2-16. Typical variation of α_N as a function of I_E for a grown-junction transistor.

volume recombination are dependent upon the width of the base region. These two recombination terms decrease as collector-base voltage is made larger. The increase in β_S causes α_N to increase, as γ_S is not significantly affected by variation of base width. For a constant drift velocity of minority carriers across the base region, less time is required to traverse the narrower base width. This reduction in base-region transit time extends the fequency response of $g(\beta)$ and gives the transistor an increased frequency range.

Variation of r_b'. Because of less-than-unity magnitudes for emitter injection efficiency and base transport factor, a current flows into the base terminal of a transistor; this current flow requires that a base resistance r_b' be included in the small-signal equivalent circuit of the device. As the effects of dc operating levels are under consideration, large-signal values are used for emitter injection efficiency and base transport factor. A decrease in either γ_S or β_S causes base current to increase, and the apparent value of r_b' decreases. Thus, the magnitude of r_b' is directly proportional to values of γ_S and β_S. In addition, the magnitude or r_b' varies directly as the resistivity of the base region and inversely as the width of the base region. Also, the magnitude of r_b' is directly proportional to the average length of transverse base-current flow. An expression for base resistance can be written.

$$r_b \propto \frac{\gamma_S \beta_S \rho_b L_a}{W} \tag{2-33}$$

where ρ_b = base resistivity
L_a = average length of transverse base-current flow
W = width of base region

At large current levels, γ_S and ρ_b tend to decrease r_b', while the β_S term has a tendency (until emitter current becomes extremely large) to increase r_b'. The L_a term of the above expression decreases at high current levels because the pinch-off effect reduces the length of transverse base-current flow. These effects cause a net decrease in r_b' as I_E is made larger.[25]

Equation (2-33) shows that r_b' is influenced by the dependence of base width upon collector-base voltage. As V_{CB} is made larger, W decreases, and r_b' increases in magnitude.

Variation of C_c. Collector capacitance is determined primarily by width of the depletion layer existing at the collector-base junction. This capacitance is not affected by the level of I_E but does vary inversely as the magnitude of V_{CB}.

Variation of r_c. Equation (2-24) shows that r_c is the limit, as ΔI_C approaches zero, of the ratio $\Delta V_{CB}/\Delta I_C$. Figure 2-13 shows that this resistance is measured at a constant level of emitter current. Because only two of three variables (V_{CB}, I_B, and I_E) are allowed to change, a partial differential equation results, and collector ac resistance can be written

$$r_c = \frac{\partial V_{CB}}{\partial I_C} \tag{2-34}$$

From Eq. (1-1),

$$I_C = \alpha_N I_E \tag{2-35}$$

Substitution of this expression into Eq. (2-34) yields

$$r_c = \frac{\partial V_{CB}}{\partial \alpha_N I_E} \tag{2-36}$$

But since I_E is now held constant,

$$r_c = \frac{\partial V_{CB}}{I_E \partial \alpha_N} \tag{2-37}$$

In order to assess the effect of the operating point upon r_c, the above expression is manipulated slightly to give

$$r_c = \frac{I}{I_E \, \partial \alpha_N / \partial V_{CB}} \tag{2-38}$$

Equation (2-38) shows that collector ac resistance is inversely proportional to the dc level of emitter current. As I_E increases, r_c decreases in a linear fashion.

The effect of V_{CB} upon r_c is determined from an analysis of the partial derivative term in Eq. (2-38). The change in α_N as a result of a change in V_{CB} is caused by variation of β_S as a function of applied voltage. Since γ_S is close to unity and only change in β_S is considered,

$$\frac{\partial \alpha_N}{\partial V_{CB}} \cong \frac{\partial \beta_S}{\partial V_{CB}} \tag{2-39}$$

The base transport factor can be expressed[13]

$$\beta_S = 1 - \frac{1}{2}\left(\frac{W}{L_B}\right)^2 \tag{2-40}$$

where L_B is the minority-carrier diffusion length in the base region. Differentiation of the above expression with respect to V_{CB} gives

$$\frac{\partial \beta_S}{\partial V_{CB}} = \frac{W \, \partial W}{L_B^2 \, \partial V_{CB}} \tag{2-41}$$

The relationship given in Eq. (2-39) allows the right side of Eq. (2-41) to be substituted into Eq. (2-38), to yield

$$r_c = \frac{1}{I_E (W/L_B^2)(\partial W / \partial V_{CB})} \tag{2-42}$$

For the grown-junction transistor,[26]

$$\frac{\partial W}{\partial V_{CB}} \propto \frac{1}{V_{CB}^{2/3}} \tag{2-43}$$

This expression can be substituted into Eq. (2-42) to give

$$r_c \propto \frac{V_{CB}^{2/3}}{I_E W / L_B^2} \tag{2-44}$$

A relationship between r_c and V_{CB} has now been established. Equation (2-44) shows that r_c increases as V_{CB} is made larger.

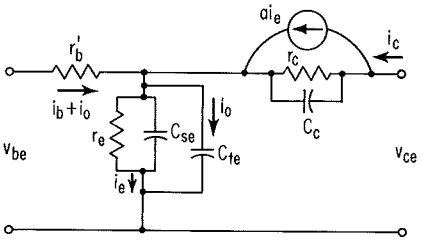

Fig. 2-17. Common-emitter small-signal equivalent circuit.

2-4. COMMON-EMITTER EQUIVALENT CIRCUIT

A small-signal equivalent circuit for the common-emitter connection is derived from the common-base equivalent circuit of Fig. 2-5. The circuit of Fig. 2-5 can be redrawn to show i_b as input current to the stage and with the emitter terminal common to both input and output portions of the circuit. This rearrangement of input terminals gives the common-emitter equivalent circuit of Fig. 2-17.

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3

Fabrication and Characteristics of Various Transistor Types

3-1. GROWN-JUNCTION TRANSISTOR

Transistor operation depends upon the presence of small amounts of N- and P-type impurities in an otherwise homogeneous crystal of semiconductor material. Successful fabrication of transistors requires that the physical location and concentration of the two types of impurity be carefully controlled.

Collector-base and emitter-base junctions of a grown-junction transistor are formed while the transistor crystal is being grown.[1] This is illustrated in Fig. 3-1, which shows various stages in the growth of a silicon crystal; N-P-N transistors

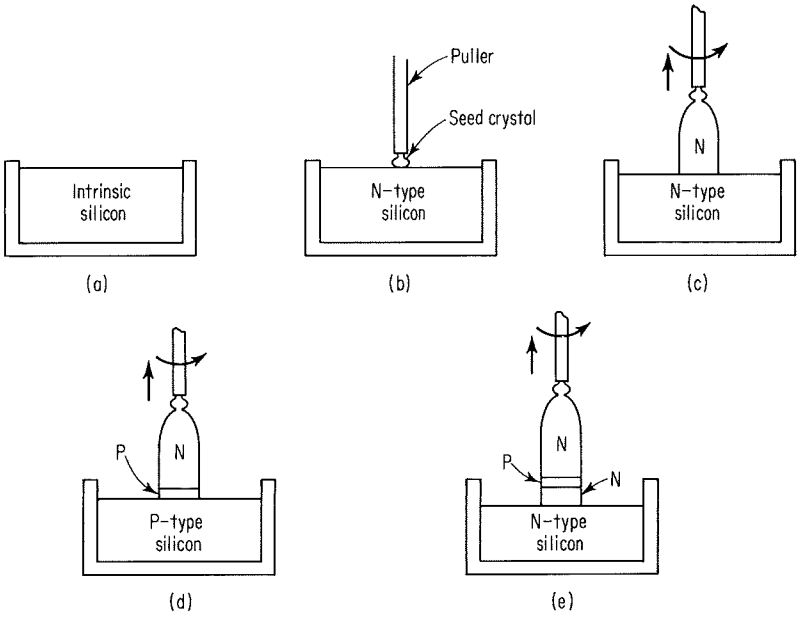

Fig. 3-1. Growth of a crystal containing layers of opposite conductivity.

are to be obtained from this crystal. Figure 3-1*a* shows a crucible containing molten silicon material. The silicon is intrinsic, i.e., it contains neither N- nor P-type impurities. In Fig. 3-1*b*, the molten semiconductor material, or melt, has been changed to N-type silicon by addition of a donor impurity such as arsenic or antimony. The degree of impurity concentration, or doping, is determined by the amount of donor material added to the melt. Figure 3-1*b* also shows a seed crystal of intrinsic silicon dipped into the melt. This seed crystal is slowly rotated as it is withdrawn. Silicon from the melt adheres to the seed crystal and solidifies, as shown in Fig. 3-1*c*. A single-crystal structure results from this pulling process. Conduction of the N-type silicon melt is changed to P-type conductivity by addition of an acceptor impurity such as gallium. This P-type impurity overcomes the donor impurities, and the melt now becomes P-type silicon. The crystal is continuously pulled, and the lower portion of the crystal is P type, as shown in Fig. 3-1*d*. After a narrow P region is grown, conductivity of the melt is changed back to N type, and the new growth of crystal has N-type conductivity as shown in Fig. 3-1*e*.

Repetition of the above process gives alternate layers of N- and P-type conductivity. The crystal is sawed into short cylinders having a P-type region sandwiched between two N-type layers. These cylinders are sawed and separated into small pieces. Figure 3-2 shows a cylinder that has been sawed, together with one of the several bars obtained from a single cylinder. Each resulting bar of semiconductor material is an N-P-N transistor, with a P-type base region and N-type emitter and collector regions. A typical bar is 120 mils in length and 17 mils in both width and height.

Each individual transistor bar is mounted on a header, and electrical connections are made to the emitter, base, and collector regions. Because of the extreme thinness of the base region, it is not possible to make electrical contact to the base without overlap into the emitter and collector regions.[2] For the N-P-N transistor, an aluminum wire of approximately 2 mils diameter is alloyed into the device, as shown in Fig. 3-3. The regrowth region is of the same conductivity as the aluminum (P-type) wire and forms a rectifying contact with the emitter and collector junctions. There is some injection directly from the emitter into the heavily doped regrowth area; recombination of minority carriers in this relatively wide region reduces forward current gain of the transistor. Extension of the regrowth area into the emitter region is made small in order to reduce emitter injection into the regrowth region.

Figure 3-4 shows a transistor bar mounted on a header and illustrates the manner in which electrical connections are made to the three regions. Collector and emitter regions are alloyed to tabs of gold-platinum alloy. These tabs are welded to bonding posts which mechanically support the transistor and electrically connect the emitter and collec-

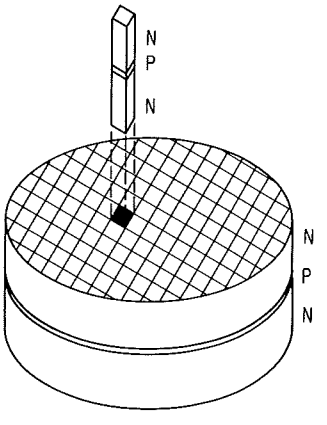

Fig. 3-2. Sawing a short cylinder yields individual bars.

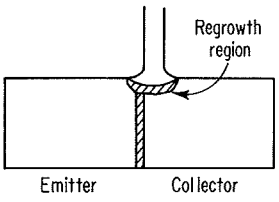

Fig. 3-3. Base wire alloyed to grown-junction transistor.

tor regions to the header. The aluminum base-contact wire is also welded to a bonding post.

A can is welded onto the header to protect the transistor from contamination, light, and physical abuse. The completed transistor is shown in Fig. 3-5.

Certain electrical characteristics of the grown-junction transistor are controlled by doping of the crystal. It is desirable that collector-base breakdown voltage of the transistor be determined by avalanche multiplication (which permits transistor action) and not by a punch-through condition. Collector resistivity of the transistor is chosen to extend the collector-base depletion layer sufficiently far into the collector region for the punch-through voltage level to be beyond that at which avalanche multiplication causes excessive collector-current flow.* Because of the lower avalanche breakdown voltage, the transistor is never subjected to the punch-through voltage level. Resistivity of the collector region is typically on the order of 2 ohm-cm, and base resistivity is nominally 1 ohm-cm. Grown-junction transistors may have $V_{(BR)CBO}$ ratings as large as 80 volts.

Reverse breakdown voltage of the emitter-base diode is typically on the order of 1 volt. Because of the heavily doped base-contact regrowth region, emitter resistivity is made extremely low (0.02 ohm-cm) in order to provide a reasonable value of emitter injection efficiency. The low-resistivity emitter region causes the depletion layer of the emitter-base junction to penetrate principally into the thin portion of the base region; hence, emitter-base breakdown voltage is low.

Equation (1-19) shows that ohmic resistance of the collector region causes an increase in $V_{CE(sat)}$. The high collector resistivity of a grown-junction transistor causes $V_{CE(sat)}$ to be as large as 1 volt for collector currents of 3 ma.

*The various other transistor types described in this chapter are also designed to have a collector-base breakdown-voltage level determined by avalanche multiplication.

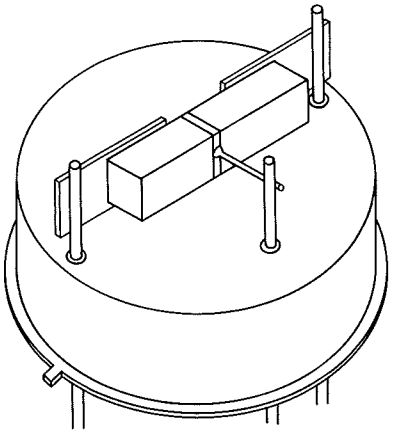

Fig. 3-4. Grown-junction bar mounted on a header.

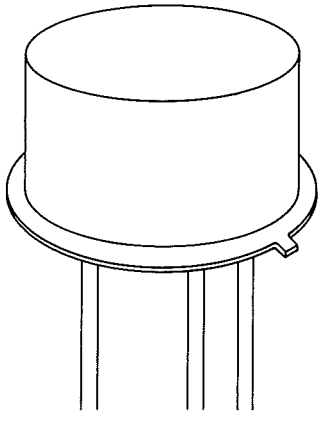

Fig. 3-5. Completed transistor assembly.

Frequency response of the grown-junction device is limited by the method of device fabrication. Base width is dependent upon the rate at which added impurities convert the melt to an opposite conductivity. Also, base width is a function of the rate at which the crystal is pulled. Reproducibility of base-layer thickness restricts the base region to a minimum thickness of approximately 0.5 mil. Alpha cutoff frequency of a grown-junction silicon structure is typically less than 10 Mhz.

3-2. ALLOY-JUNCTION TRANSISTOR

Historically, the grown-junction transistor was the first junction device. The second form of junction transistor to be developed was the alloy-junction transistor.[3] This type, which is widely used today, is formed by alloying two dots, or pellets, to both sides of a thin piece of semiconductor material. The fabrication process of a germanium P-N-P alloy-junction transistor is described below. An N-P-N alloy-junction device is made in a similar manner.[4]

A single-resistivity N-type germanium crystal is grown and sawed into thin slices of approximately 20 mils thickness. These slices are lapped to remove saw marks and then polished. The individual slices are cut into small rectangular or circular wafers. Each wafer eventually becomes the base region of a transistor.

Collector and emitter regions of the transistor are formed by alloying pellets, or dots, of P-type impurity—indium in this case—into the N-type germanium wafer. This is illustrated in Fig. 3-6, which shows four stages in fabrication of the alloy-junction device. In Fig. 3-6*a* the indium pellet is placed atop the N-type wafer. The two materials are then subjected to heat, and the indium begins to melt. Germanium is dissolved in the indium, and the germanium-indium interface penetrates the surface of the wafer. Upon cooling, germanium recrystallizes, again becoming a part of the original crystal structure. However, this recrystallized germanium now contains a sufficient amount of indium for its conductivity to have changed to P type. The alloyed dot is shown in Fig. 3-6*b*, and Fig. 3-6*c* shows a second, smaller, indium dot placed on the other side of the germanium wafer from the alloyed pellet. This smaller pellet is shown in Fig. 3-6*d* to be alloyed into the wafer and to form a second P-N junction. The alloying process causes a small amount of indium to flow across both surfaces of the wafer and to form a short-circuit path between the two indium pellets. This thin covering of indium is removed by an acid etch.

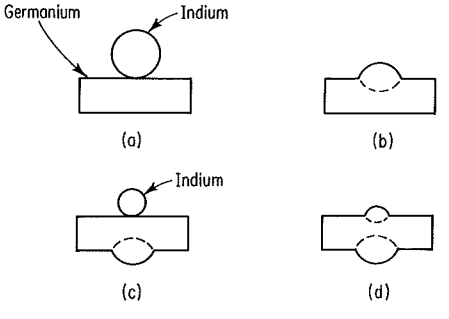

Fig. 3-6. Stages in fabrication of alloy-junction transistor.

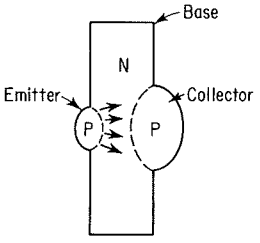

Fig. 3-7. Hole current flow through base region of alloy-junction transistor.

Alloy-junction transistors are usually fabricated by the "batch process," i.e., dots are alloyed into many wafers at a single step. Wafers of like thickness are selected for a particular batch, and alloying time is adjusted for the thickness of these wafers. In this manner, alloy-junction transistors of nearly identical electrical characteristics can be obtained from wafers of varying degrees of thickness.

Figure 3-7 shows the alloy-junction structure, together with several paths of hole current flow in the N portion of the device. For each of the two alloyed regions, the P-N junction exists at the dotted line. Alloying occurred only at the dotted lines, and the remaining pure indium serves as low-resistance metallic contacts for the two junctions.

Unequal collector and emitter areas have been designed into the alloy-junction structure shown in Fig. 3-7. The larger of the two alloyed indium pellets is taken as the collector terminal, with the other pellet designated as the emitter terminal. In the base region, formed by the original germanium wafer, emitter-injected holes follow divergent paths, as shown in the figure. The collector-junction area is made relatively large in order to collect as many of these holes as possible. If the smaller alloyed dot were to be used as the collector terminal, with the other dot serving as the emitter terminal, many of the injected holes would not be captured, and current gain of the transistor would be considerably lower than when the collector and emitter terminals are used as collector and emitter, respectively.

Resistivity of the indium dots is on the order of 0.001 ohm-cm. At the collector

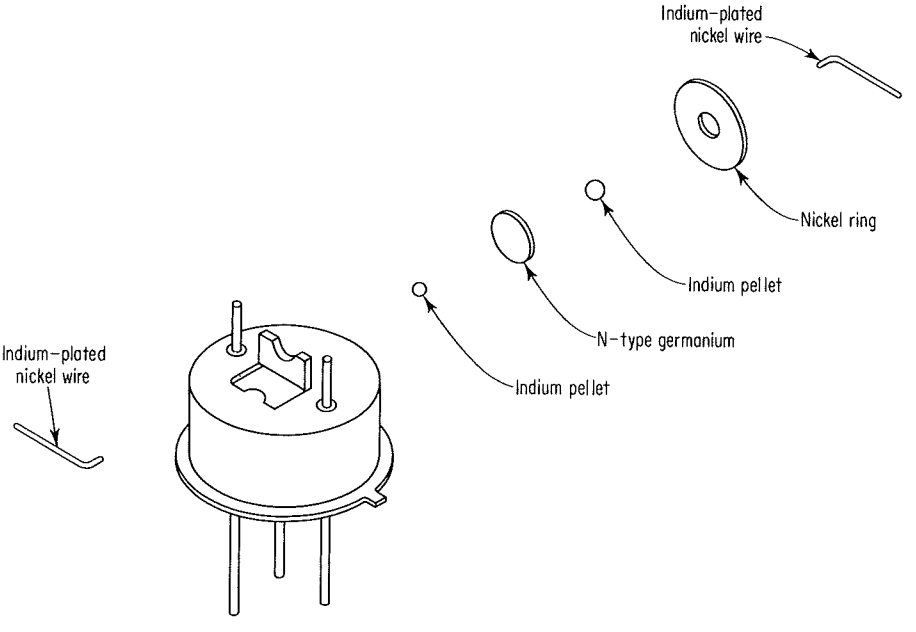

Fig. 3-8. Elements of a P-N-P alloy-junction transistor.

and emitter junctions, the P-type resistivities are determined by the amount of indium dissolved in the recrystallized germanium and are considerably larger than the resistivity of the pure indium metal. Resistivity of the base region is typically 1 to 2 ohm-cm. Breakdown voltages $V_{(BR)CBO}$ and $V_{(BR)CEO}$ are approximately equal and are usually limited to a maximum value of approximately 30 volts. The small ohmic resistance of the collector region gives low saturation-voltage drops at moderately large levels of collector current. At a collector current of 10 ma, $V_{CE(sat)}$ may have a typical value of 0.1 volt.

Large-scale fabrication of alloy-junction transistors limits base-region thickness to a minimum value of approximately 0.5 mil. Germanium alloy-junction devices may have alpha cutoff frequencies as large as 20 Mhz.

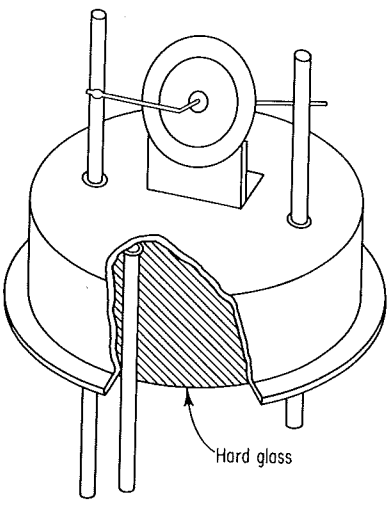

Fig. 3-9. Alloy structure connected to header.

Figure 3-8 shows the elements of an alloy-junction transistor and illustrates one manner in which the active device is mounted and contacted. A nickel ring is used to support the germanium wafer. Figure 3-9 shows the active device connected to the header. The nickel ring is welded to the support tab on the header and provides an electrical connection between the base and header. The cutaway view shows a hard glass used for support and electrical isolation of the three leads extending below the header. Two of the leads pass through glass beads into the header; the third lead is butt-welded to the header shell in order to make electrical contact to the base region. The two indium-plated nickel wires are resistance-welded to the bonding posts and are fused, by application of heat, into the indium pellets. A can is welded onto the lower flange to complete the fabrication process.

3-3. GRADED-BASE TRANSISTORS

Diffusion of minority carriers through the base region was described in Sec. 2-2. At low levels of collector current, this diffusion mechanism was seen to be the principal method of carrier transport through the base region. It was pointed out in Sec. 2-3 that at high levels of collector current an electric field exists within the base region and produces a drift velocity of the minority carriers. This drift component of velocity adds to the original diffusion velocity and reduces base-region transit time of the minority carriers.

Advances in the understanding of transistor physical operation, as well as improved techniques in the preparation of semiconductor materials, have led to fabrication processes which provide a "built-in" electric field within the base region.[5] This electric field is the result of a variation in impurity concentration over the base width. Concentration of base-region impurities, or majority carriers,

is controlled by diffusing opposite-type impurities into a doped piece of semiconductor material. This diffusion can be either a gaseous or a liquid process.* Figure 3-10 shows a bar of P-type semiconductor material into which an N-type impurity has been diffused. Donor impurities have diffused to the right and have overcome the original P-type conductivity of the bar within the length d; the bar now contains two regions of opposite conductivity. Because the diffusion process began at the left edge of the bar, the N-type impurity concentration varies from a maximum at this edge to a minimum at distance d within the bar. The lower part of Fig. 3-10 shows a typical plot of electron gradient within the N-type region. This nonuniform distribution of carriers produces an electric field within the N-type region, which accelerates minority carriers to the right. If this region is used as the base of a transistor, the electric field will aid the transport of minority carriers through this region.

A P-type region can be added to the left of the N-type region in the above figure to give a transistor structure. The original P-type region serves as the collector region, with the P-type structure to the left serving as the emitter portion of the device. Graded-base transistors are fabricated to have a base-region concentration which varies from a maximum at the emitter junction to a minimum at the collector junction.

In addition to giving an increased frequency response, the graded-base region reduces r_b' and C_c of a transistor structure. The larger impurity doping at the emitter edge of the base region causes average base resistivity to be below that of the non-graded-base device. The nonuniform distribution of majority carriers in the diffused-base structure gives a relatively high base resistivity at the collector edge of the base region; the collector-base depletion layer now extends farther into the base region, and collector transition capacitance is reduced.

Control of base-region thickness in the grown-junction and alloy-junction devices is not adequate for economical mass production of extremely thin base regions in either of these transistor types. The base region of a grown-junction transistor is formed in approximately 5 to 10 sec. Alloying of emitter and collector dots to define the base region of the alloy-junction device is also performed in only a few seconds. Because of the short time available to form the base region in either the grown- or alloy-junction devices, and also because of slight variations in material, temperatures, and certain mechanical aspects of the various operations, a semiconductor manufacturer usually does not strive for base-region thickness of less than approximately 0.5 mil for either the grown- or alloy-junction devices.

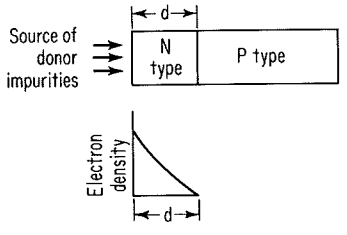

Fig. 3-10. Impurity diffusion into P-type semiconductor.

A diffused-base structure, however, permits ready fabrication of narrow base widths. The diffusion process may require from 20 min to several hours, depending upon the temperature at which diffusion takes place. Time and tempera-

* The diffusion process referred to here is the diffusion of atoms into a solid material and is not to be confused with the diffusion mechanism of minority-carrier flow in the transistor.

ture can be adjusted to give precise control over the diffusion of impurities into a semiconductor material.[6,7] Base widths as small as 2×10^{-5} in. are well within the limits of present fabrication technology.

Diffusion techniques can be incorporated in the fabrication processes of both the grown-junction and alloy-junction devices.[8-10] However, as the diffused-base versions of these device types find little use in present-day transistor switching circuits, they are not considered further. Two newer device types, the mesa transistor and planar transistor, depend upon a diffused-base structure for their operation and are widely used in transistor switching circuits. These two transistor types are considered in detail in the next two sections.

3-4. MESA TRANSISTOR

Various forms of diffused-base transistors have evolved. One method of construction yields diffused-base transistors which, because of their physical appearance, are generally referred to as "mesa transistors."[11] Fabrication of a P-N-P germanium mesa transistor is described below, and certain electrical characteristics of the device are discussed.

As a first step in fabrication of the mesa transistor, N-type impurities are diffused into a slice of single-resistivity P-type germanium. The diffusion furnace used to perform this part of the process consists, typically, of an electrically heated glass tube having a temperature-controlled heat zone. The glass tube contains a gaseous form of the N-type diffusant, say antimony. The germanium slice, which has been lapped and polished, is placed within the constant-temperature heat zone of the furnace. As a result of gaseous diffusion of antimony into the germanium slice, a thin skin of N-type conductivity forms over the slice as shown in the cross-sectional view of Fig. 3-11. There has been no change in original dimensions of the slice, as the impurity has diffused *into* the slice. Several transistors are to be obtained from this slice. The remaining fabrication steps yield repetitive patterns of transistors on the slice.

An evaporation technique is next used to place emitters across one surface of the slice. Emitter areas are defined by a metal mask of the type shown in Fig. 3-12. This mask, which contains several rectangular openings, is placed over one surface of the diffused slice. The mask and slice are inserted in a vacuum chamber, and a small amount of aluminum is placed above the mask. A vacuum is created within the chamber, and the aluminum is heated to a gaseous state. Evaporated aluminum is able to strike the slice only through the openings in the metal mask;

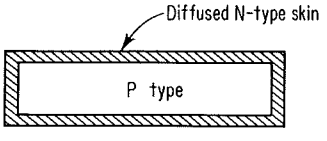

Fig. 3-11. N-type skin diffused into P-type wafer.

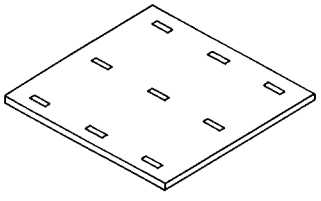

Fig. 3-12. Metal mask for depositing emitter and base stripes.

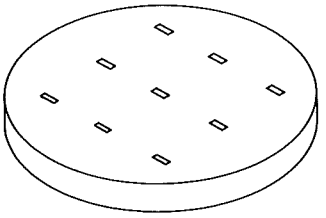

Fig. 3-13. Aluminum stripes evaporated upon diffused slice.

consequently, narrow stripes of aluminum are deposited across the surface of the diffused slice. Figure 3-13 shows aluminum stripes evaporated upon the diffused slice. Heat is next applied to the slice, and the aluminum stripes alloy into the diffused N-type skin. Aluminum has P-type conductivity, and each alloyed aluminum stripe becomes a P-type emitter.

Ohmic contacts are next made to the N-type diffused layer. The metal mask described above remains over the slice but is indexed slightly so that the rectangular openings lie alongside, and parallel to, the aluminum stripes. Gold is then evaporated upon the slice, and the resulting gold stripes are fused into the N-type skin.

Each pair of aluminum and gold stripes, together with the original P-type germanium, forms a P-N-P transistor. The aluminum stripe is an emitter, and the gold stripe serves to make contact to the N-type base region. The collector region is next exposed, and a small collector-base region is provided.

A photoetching technique is used for selective removal of part of the N-type diffused layer. The top surface of the slice, including the aluminum and gold stripes, is covered with a photosensitive emulsion. A glass mask containing square-shaped clear areas is placed over the emulsion and aligned so that each pair of emitter and base stripes is within a clear area of the mask. Figure 3-14 shows cross-sectional side views of the slice during various stages of the remaining fabrication process. Figure 3-14*a* shows the glass mask aligned over the base and emitter stripes. Ultraviolet light is shone upon the glass mask to expose the emulsion directly under the clear areas of the mask. Those portions of emulsion which have been exposed to light are now polymerized. An etch solution which

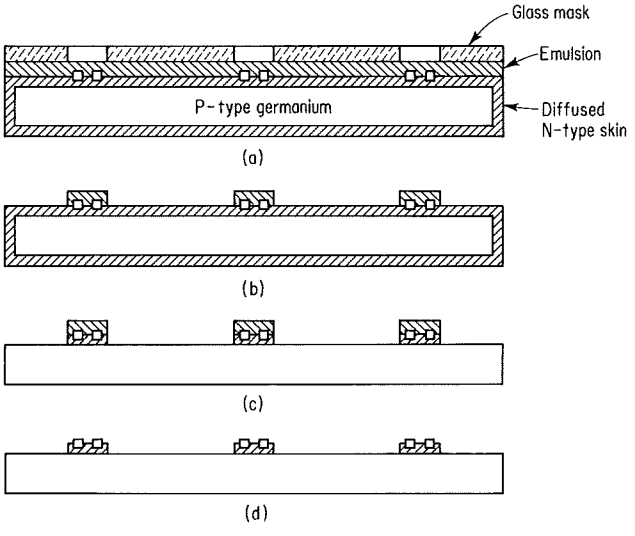

Fig. 3-14. Cross-sectional view of slice during various stages of processing.

dissolves only nonpolymerized emulsion is applied to the slice, and the portions of unexposed emulsion are removed. Figure 3-14*b* shows the islands of emulsion which now remain. The slice is then placed in an etch solution which dissolves germanium but not the remaining emulsion. The N-type diffused layer is selectively removed and remains only where it is protected by emulsion. Figure 3-14*c* shows the slice after etching of the N-type layer. The slice is then placed in an etch solution which removes only the remaining emulsion. Figure 3-14*d* shows the slice after this final etch process.

Each of the raised areas in Fig. 3-14*d* resembles a mesa. A diamond scribe is next used to cut shallow channels between adjacent mesas. This simplifies breaking the slice into small wafers, with each wafer containing one mesa transistor. Figure 3-15 shows the mounted transistor, together with connecting wires from the emitter and base stripes to the two bonding posts. These wires are bonded, by application of heat and pressure, to the two posts and the two stripes. A gold solder is used to mount the collector portion of the transistor onto the header. One external lead is electrically connected to the header and serves as the collector lead of the assembled transistor. A can is soldered onto the header to complete fabrication of the mesa device.

For the typical mesa structure, emitter and base stripes are each 3 mils by 1 mil and are separated from each other by a distance of 1 mil. The mesa area is typically a 4-mil square. The small area of the evaporated emitter stripe gives a low value of C_{te}, and the small mesa area is responsible for a low value of C_{tc}.

Collector resistivity of the mesa transistor is chosen sufficiently large to allow the avalanche effect to determine collector-base breakdown voltage; this breakdown voltage is typically at least 15 volts. Ohmic resistance of the collector region causes $V_{CE(\text{sat})}$ of the mesa transistor to be approximately twice as large as that of the alloy-junction device but still considerably lower than that of the grown-junction transistor.

A low emitter resistivity, together with a thin base region, gives the mesa device a low $V_{(BR)EBO}$ value, typically on the order of 1 to 3 volts.

Base-region charge-storage effects of the saturated mesa device are negligible. Transit time of carriers through the narrow base region is extremely small, and any stored minority carriers are quickly removed. In addition, those base-region minority carriers which are injected from the collector face an electric field which tends to force them back into the collector region.

There may be a significant amount of stored charge in the collector region of a saturated mesa transistor. When the collector-base junction is forward-biased, the low-resistivity base injects many carriers into the high-resistivity collector. These carriers, which are minority carriers in the collector region, flow toward the

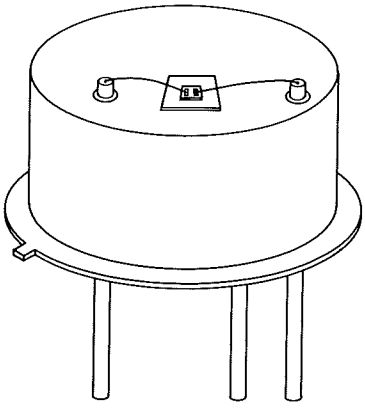

Fig. 3-15. Mesa structure connected to header.

collector terminal. There is little recombination of these carriers because of high resistivity of the collector region. When the collector-base junction is no longer forward-biased, the minority carriers must either recombine in the collector or be drawn back into the base region. The collector region is typically 3 to 4 mils wide, and transit time of minority carriers back to the base region is usually appreciable with respect to the switching speeds at which the mesa transistor is employed.

Gold is sometimes used to reduce the lifetime of minority carriers in the collector region. The gold provides recombination centers, which reduce carrier lifetime by providing excess holes or electrons to recombine with the carriers.[12] Lifetime reduction by gold is greater for holes than for electrons. For this reason, gold is more widely used in N-P-N transistors than in P-N-P transistors. The gold is diffused into the collector region, usually before or during base-region diffusion.

To a large extent, the starting semiconductor material determines whether alloying or diffusion is used to form a junction. Germanium is well suited to alloying, whereas silicon is better suited to a diffusion process. A diffused emitter structure is used for silicon mesa transistors, as contrasted to the alloyed emitter of the germanium mesa device. The diffused emitter structure of a silicon mesa transistor provides a graded emitter having a higher resistivity at the base junction than would be obtained with an alloyed emitter. The silicon mesa transistor has a typical $V_{(BR)EBO}$ of approximately 5 volts; this is considerably larger than the $V_{(BR)EBO}$ of the germanium mesa device.

Figure 3-16 depicts various stages in fabrication of a diffused silicon mesa tran-

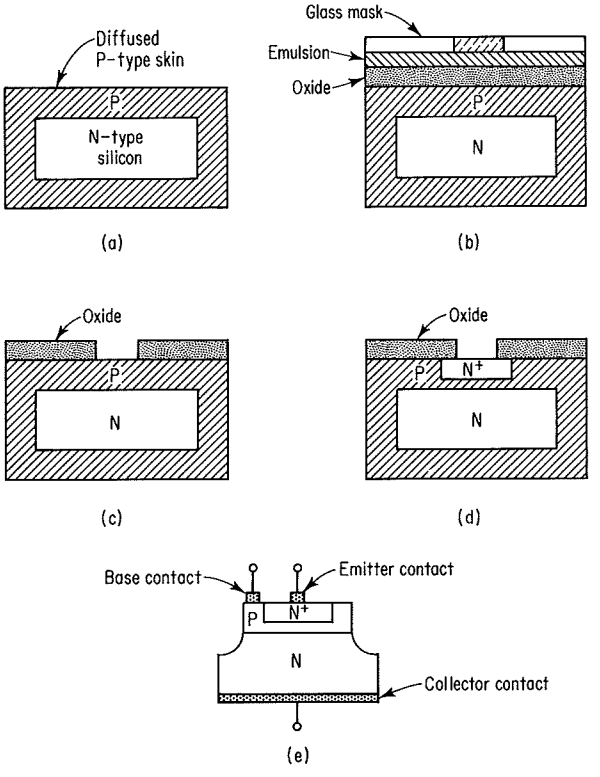

Fig. 3-16. Various stages in fabrication of a diffused silicon mesa transistor.

sistor. Although many transistors are fabricated simultaneously on a slice, only a single transistor is considered in the following discussion; the figure shows cross-sectional views of a single wafer. Figure 3-16*a* shows the N-type wafer with a diffused P-type skin. An oxide is grown over the top surface of the wafer, and a photosensitive emulsion is spread over the oxide. A glass mask is placed over the emulsion; Fig. 3-16*b* shows the wafer at this stage of fabrication. The emulsion is exposed and etched in the manner described for the germanium mesa-fabrication process. The opaque section of the mask causes a window to be cut in the emulsion. The wafer is placed in a solution which removes exposed oxide, and a window is opened in the oxide. The emulsion is removed and the wafer looks as shown in Fig. 3-16*c*. Continuing further, the wafer is next subjected to a gaseous N^+-type diffusion. The N^+-type impurities diffuse down and sideways into the P-type impurity and form a diffused-emitter structure; Fig. 3-16*d* shows the wafer after passing through this diffusion step. Oxide is next removed, a mesa is etched, and the excess P-type diffusion is removed. Figure 3-16*e* shows the completed transistor. The ohmic contacts are actually made to a transistor header of the type shown in Fig. 3-15. A transistor having both a diffused base and a diffused emitter is often classified as a "double-diffused transistor."

3-5. PLANAR TRANSISTOR

An extension of the photomasking, etching, and diffusion techniques described above can be used to diffuse both the base and emitter regions through windows in an oxide covering. The process for achieving this structure is somewhat similar to that already described for emitter diffusion, except that a base region is first diffused through a window in the oxide. After base diffusion, the oxide is re-grown, and a second window, smaller than the first window, is opened above the base diffusion. An emitter is diffused through this window. The remaining oxide is selectively removed in order to make ohmic contact to the base region. Emitter and base contacts are formed by evaporating a metal, say aluminum, over the oxide and selectively removing, by photomasking and etching, unwanted portions of the metal. Figure 3-17*a* shows a cross-sectional view and Fig. 3-17*b* a top view of the completed transistor. The large metal areas in Fig. 3-17*b* serve as pads to which gold wires are bonded. These wires are also bonded to posts on a transistor header. Ohmic contact is made to the collector region in the same manner as for the mesa transistor.

An oxide layer covers the three junctions of a planar device and significantly reduces surface components of leakage currents.[13] This protective oxide covering causes the planar structure to have an I_{CBO} level considerably below that of all other device types. In addition, surface recombination is reduced, and low-level current gain is increased.

Frequency response of a transistor is determined by the physical size of the emitter, base, and collector regions. For any transistor, a lower limit is imposed on device size by the necessity of making ohmic contact to the above three regions. Emitter and base stripes of a mesa transistor must be sufficiently large to accommodate the gold wires connected to them. Planar geometry allows the use of evaporated metal contacts to the emitter and base junctions. These contacts can

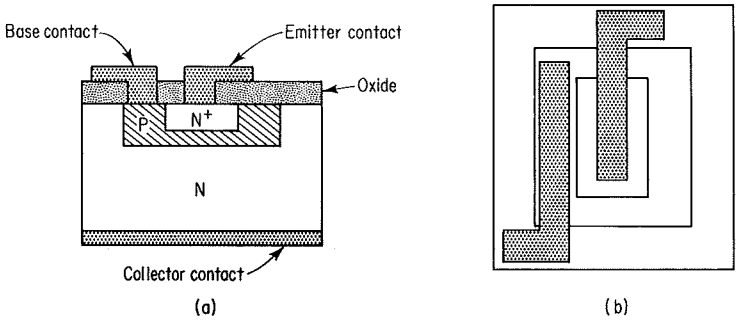

Fig. 3-17. Planar transistor. *(a)* **Cross-sectional view;** *(b)* **top view.**

be made to a much smaller area than is required for a bonded gold wire. The metal pattern can provide suitable pads, as shown in Fig. 3-17, to which gold wires may be bonded. This technique of "expanding" the emitter and base contact areas permits small-geometry base and emitter regions to be fabricated and, for a given starting material (silicon or germanium), enables a planar transistor to have a higher frequency response than a mesa device.

3-6. EPITAXIAL TRANSISTORS

In general, transistor design involves a compromise among certain of the electrical characteristics. Base resistivity must be high, relative to emitter resistivity, to provide an adequate value of emitter injection efficiency. A large base resistivity also serves to increase base transport factor. As base resistivity increases, punch-through voltage level of the collector-base junction decreases. Collector resistivity must be chosen to give a reasonable magnitude of punch-through voltage and yet not cause excessive ohmic resistance of the collector region. Frequency response of a transistor is determined principally by base width. High-frequency devices are designed to have a narrow base region at the expense of reduced reverse-breakdown-voltage ratings of the collector-base and emitter-base junctions.

Attempts to maintain a low collector bulk resistance by increasing collector resistivity and correspondingly reducing thickness of the collector region are not useful for the mesa and planar structures. If collector thickness is made too low, the devices become fragile and are easily broken. A low-resistance collector region can be obtained, however, while maintaining a high collector resistivity at the collector-base junction, by use of epitaxial deposition.[14,15] This deposition forms a film of semiconductor material upon the surface of a slice of germanium or silicon. Crystal orientation of the epitaxial layer follows the same crystal orientation as that of the substrate material. Resistivity of the epitaxial layer may be considerably different from that of the substrate material.

Figure 3-18 shows a cross-sectional view of an epitaxial P-N-P mesa transistor. The collector region of this device consists of the P^+ starting material and the P-type epitaxial layer. Resistivity of the epitaxial layer is fairly high, and collector resistivity at the collector-base junction is considerably larger than that of a non-epitaxial device. Collector resistance of the epitaxial transistor is determined

principally by the P^+ substrate; this gives a low value for total collector resistance.

Compared to a nonepitaxial device having the same geometry, the epitaxial transistor described above has a large punch-through voltage rating and, typically, less than one-half the $V_{CE(sat)}$ magnitude for given conditions of base and collector currents. Low bulk resistance of the epitaxial transistor gives the collector a good injection efficiency when the collector-base junction becomes forward-biased. Since the base does not inject many carriers into the collector region, the adverse effect of minority-carrier lifetime in the collector region is minimized. Although collector injection into the base is now larger than for the nonepitaxial device, base-region storage effects are still small.

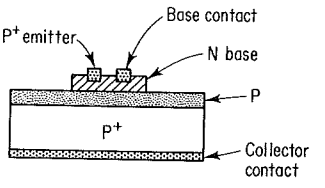

Fig. 3-18. Cross-sectional view of an epitaxial P-N-P mesa transistor.

Depletion-layer capacitance of the collector-base junction is reduced by the high-resistance expitaxial layer. Extension of the depletion layer farther into the collector region results in a wider depletion layer and a smaller magnitude of C_{tc}.

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4

The Transistor as a Switch

4-1. INTRODUCTION

Various types of computer and control operations can be performed with switches which have two distinct levels of output current or voltage. In electrical circuits, these switches may be relays, manual switches, or electronic switches. Relays and manual switches, when closed, have forward-voltage drops on the order of a few millivolts or less. When open, these switching elements offer a resistance to current flow of several megohms, depending upon leakage paths between switching contacts. The electronic switches described in this book are the transistor and the diode. These two devices, compared to the relay and manual switch, offer less impedance to the flow of current when turned off and have a larger forward voltage drop when turned on. Two advantages of these electronic switches are their speed of operation and their lack of moving parts. The purpose of this chapter is to examine the transistor as a switch and to indicate factors affecting on and off currents and voltage levels. Also to be considered is speed or response of the transistor in changing from one state to another.

4-2. TRANSISTOR SYMBOLS AND BASIC CIRCUIT CONNECTIONS

In order to discuss physical operation of the transistor, it has been convenient to represent a transistor as a bar containing two N regions and one P region (for the N-P-N device). This somewhat pictorial representation is generally similar to the actual physical appearance of a grown-junction transistor (although relative proportions of base, emitter, and collector regions are not accurately shown). This type of symbol is useful for analyzing transistor operation and is often used in circuit schematic diagrams. More widely used schematic representations for the N-P-N and P-N-P transistors are shown in Fig. 4-1*a* and *b*, respectively. The emitter lead of each transistor type is seen to have an arrowhead which points in the direction of conventional current flow in the emitter lead.

Transistors have three terminals and may be connected into a circuit in one of several different configurations. Input connections may be made to any two terminals, with the output appearing across the third terminal and one of the input

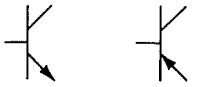

Fig. 4-1. Transistor symbols.

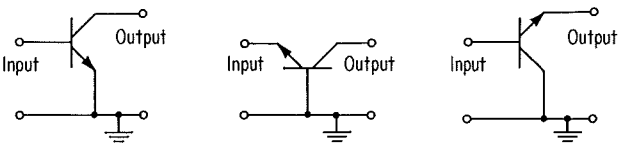

Fig. 4-2. Basic circuit configurations.

terminals. Figure 4-2 shows three basic circuit configurations. Circuits shown in Fig. 4-2*a* to *c* are designated common-emitter, common-base, and common-collector (or emitter-follower) circuits, respectively. When the common input-output terminal is connected to ground potential, as shown in the figure, the three circuit configurations are often referred to as grounded-emitter, grounded-base, and grounded-collector circuits, respectively.

Various modifications can be made to the three basic circuit configurations. One such modification is to connect an impedance between ground potential and the common element. When this is done, circuit operation may differ considerably from operation with the common element grounded.

4-3. BASIC TRANSISTOR SWITCHING CIRCUITS

It is not necessary that the transistor turn completely on or completely off in order to provide the two distinct signal levels referred to in Sec. 4-1. However, a large number of transistor switches do operate in this manner. Also, an understanding of this type of operation provides a background for an analysis of various other modes of transistor switching operation. For these two reasons, the switching circuits considered in this chapter are of the type in which the transistor is in saturation when ON and at, or close to, collector-current cutoff when OFF.

The grounded-emitter and grounded-base switching circuits can be made to operate from saturation to cutoff and are discussed in this section. The grounded-collector switch is usually designed to operate out of saturation and is discussed in a later chapter.

Common-emitter Switch. A simple transistor switching circuit is shown in Fig. 4-3. The input signal varies between ground potential and V_1 as shown. A loop equation can be written for that portion of the circuit comprising the collector supply voltage, load resistor, and transistor to give*

$$V_{CC} - I_C R_L - V_{CE} = 0 \tag{4-1}$$

This equation shows that if there were no voltage drop across the transistor, the collector current would become

$$I_C = \frac{V_{CC}}{R_L} \tag{4-2}$$

* Collector leakage current is considered to be negligible.

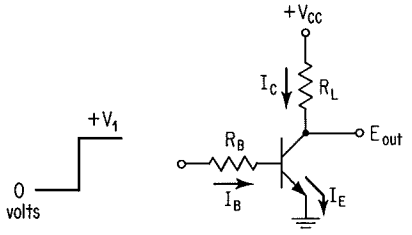

Fig. 4-3. Common-emitter switch.

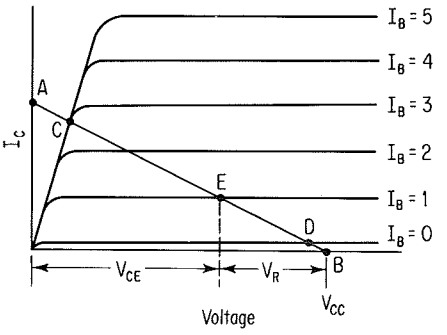

Fig. 4-4. Operating curves of switch.

Conversely, if collector current were equal to zero, there would be no voltage drop across R_L and, from Eq. (4-1),

$$V_{CE} = V_{CC} \tag{4-3}$$

when the transistor is at cutoff.

Operation of the circuit of Fig. 4-3 is explained with the aid of the transistor collector characteristic curves given in Fig. 4-4. These curves, which show the relationship between base-current, collector-current, and collector-emitter voltage, were discussed in Chap. 1. The magnitude of collector current indicated in Eq. (4-2) and the collector-emitter voltage given in Eq. (4-3) are plotted in Fig. 4-4 as points A and B, respectively. Equation (4-1) can be solved for I_C to give

$$I_C = -\frac{1}{R_L} V_{CE} + \frac{V_{CC}}{R_L} \tag{4-4}$$

This is the equation of a straight line having a slope of $-1/R_L$ and a vertical axis intercept of V_{CC}/R_L. The points A and B are at the two ends of this line and show the position and slope of the line. The line connecting A and B determines a particular relationship between input and output currents of the transistor and collector-emitter voltage drop of the device. This line is often referred to as the load line of the circuit. At any operating point along the load line, the sum of V_{CE} and V_R (the voltage drop across R_L) is equal to the voltage V_{CC}. The figure shows relative magnitudes of V_{CE} and V_R for the $I_B = 1$ base drive.

When the input voltage of Fig. 4-3 rises to V_1, current flows into the base terminal of the transistor, and the device is turned on. Collector-current magnitude is determined from Fig. 4-4 by the value of base current and position of the load line. In order for the transistor to be in saturation when in the ON state, an adequate magnitude of base current must be supplied to cause the circuit to operate at point C. The figure shows that base currents at least as large as the $I_B = 3$ curve will cause saturation. Current flow into the base terminal of Fig. 4-3 is considered a turn-on, or forward current, and is determined by the value of V_1, the base input circuit, and the magnitude of base-emitter voltage drop. The

turn-on base current is often designated by the symbol I_{B1} and can be expressed*

$$I_{B1} = \frac{V_1 - V_{BE(ON)}}{R_B} \tag{4-5}$$

where $V_{BE(ON)}$ is the voltage drop of the forward-biased base-emitter junction.

If the voltage V_{CC} were applied directly to the collector of the transistor, collector current would rise to the value $\beta_N I_{B1}$. However, the maximum value of collector current which can flow in the circuit is limited by R_L and is determined from Eq. (4-1) to be

$$I_{C(max)} = \frac{V_{CC} - V_{CE(sat)}}{R_L} \tag{4-6}$$

where V_{CE} has been replaced by $V_{CE(sat)}$, the collector-emitter voltage drop of the saturated transistor. In order for the ON state of the transistor to be at point C of Fig. 4-4, the base-input network is designed to give sufficient base current so that

$$\beta_N I_B > I_{C(max)} \tag{4-7}$$

This expression indicates that more than enough base current is to be supplied for the amount of collector current which can flow, and consequently the transistor will be in saturation.

The curves of Fig. 4-5 are an expanded section of the curves of Fig. 4-4 in the region of point C and show that the value of $V_{CE(sat)}$ is dependent upon base current to the transistor. Although $V_{CE(sat)}$ is often less than 200 mv for transistors operating at collector currents as large as 100 ma, this voltage drop is not negligible. Thus, the saturated transistor has considerably more forward-voltage drop than either the relay or manual switch.

When the input voltage in Fig. 4-3 falls to ground potential, the transistor base is connected to ground through a resistor; the transistor is at cutoff, collector leakage current is equal to I_{CER}, and the quiescent operating point of the circuit is at point D of Fig. 4-4.† The collector characteristic curves show that although the transistor is off, it does not present an infinite impedance to current flow in the circuit. The magnitude of collector leakage current is dependent upon operating temperature of the transistor and the value of series resistance in the base circuit. At room temperatures and under normal operating conditions, this current is usually less than 10 μa for even medium-power transistors and can safely be neglected in many circuit designs.

Consider now the relationship between input- and output-voltage levels in the circuit of Fig. 4-3. Output voltage of the circuit is measured with

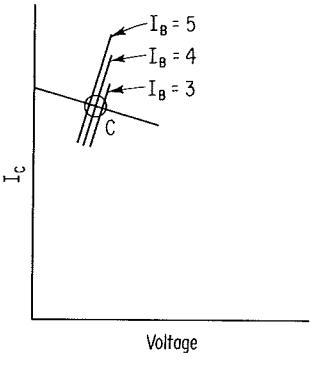

Fig. 4-5. Expanded region of collector curves to show dependence of $V_{CE(sat)}$ on base drive.

* Equation (4-5) is valid only for $V_1 \geq V_{BE(ON)}$.

† See Sec. 1-8 for a discussion of collector leakage current.

respect to ground potential and is equal to the collector-emitter voltage of the transistor. If Eq. (4-1) is solved for V_{CE} and the symbol E_{out} substituted for V_{CE}, the following relationship is obtained:

$$E_{\text{out}} = V_{CC} - I_C R_L \tag{4-8}$$

For the base-input signal at ground potential, only a small collector leakage current flows, and the collector voltage is close to the V_{CC} potential. As the base-input voltage rises to a positive level, collector current flows, and there is an increased voltage drop across the collector load resistor. This voltage drop subtracts from the collector supply voltage, and the collector-emitter voltage is lower than for the condition of zero input-signal level. The maximum positive level of base-input signal causes the collector-emitter voltage to be at its minimum value. Thus, the transistor switch of Fig. 4-3 *inverts* an input signal and is properly referred to as an "inverter." Inversion is always obtained when the transistor operates as a grounded-emitter switch.

Modified-common-emitter Switch. The preceding analysis of the common-emitter switching circuit considered the external signal appearing at the base terminal to be the controlling, or input, signal of the circuit. A positive-level input signal to the circuit of Fig. 4-3 causes the base to be positive with respect to the emitter. Thus, when the input signal becomes positive, the emitter is negative with respect to the base. An equivalent input-circuit configuration can be obtained by grounding the external base resistor and applying a negative-level input signal to the emitter terminal. This circuit configuration is shown in Fig. 4-6 and will be referred to as a "modified-common-emitter switch;" the collector external circuit remains the same as for Fig. 4-3.

Base current for the circuit of Fig. 4-6 is determined from Eq. (4-5). When the input signal is at ground potential, the transistor is at cutoff, and the output voltage is approximately equal to V_{CC}. As the input voltage increases in magnitude to $-V_1$, the transistor turns on and, if adequate base current flows, the transistor saturates. The output signal appears at the collector terminal. Collector voltage at saturation is given as

$$E_{\text{out}} = -V_1 + V_{CE(\text{sat})} \tag{4-9}$$

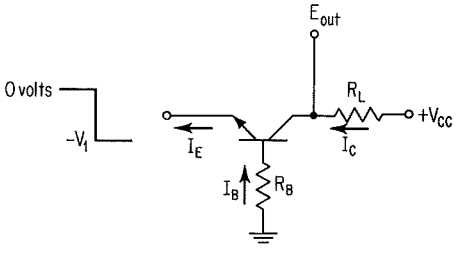

Fig. 4-6. Modified-common-emitter switch.

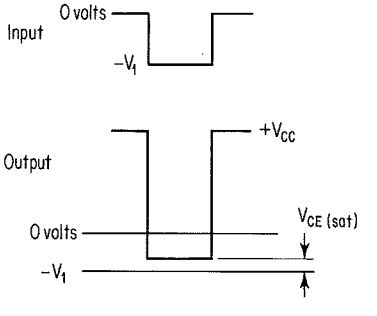

Fig. 4-7. Input and output waveforms for circuit of Fig. 4-6.

Figure 4-7 gives the relationship between input and output signals for this circuit and shows that the two signals have the same relative polarities. It is interesting to note that the output voltage varies above and below ground potential.

When the transistor in Fig. 4-6 is turned on, the saturated collector current is given as

$$I_{C(\max)} = \frac{V_{CC} + V_1 - V_{CE(\text{sat})}}{R_L} \tag{4-10}$$

Because a portion of the emitter current flows from the base terminal, the collector current is slightly less than the input current, and the circuit current gain is less than 1. In order for the transistor to be saturated, sufficient emitter current must be supplied to give the value of I_C determined from Eq. (4-10). Base-current magnitude can easily be determined from Eq. (4-5). If the value of base current is sufficient to satisfy the inequality of Eq. (4-7), the transistor is saturated, and emitter current is at the required magnitude. Thus, although the input signal is applied to the emitter terminal, the design analysis is simplified if base current is considered to be the controlling current.

Common-base Switch. Figure 4-8 shows a common-base transistor configuration in which the input signal is applied to the emitter terminal and base current is limited by an emitter resistor. When the transistor is in saturation, collector voltage is only slightly more negative than the base potential. The output voltage will now vary between V_{CC} and a small negative-voltage level.

Collector current required for saturating the transistor in Fig. 4-8 is given as

$$I_{C(\max)} = \frac{V_{CC} + V_{CB(\text{sat})}}{R_L} \tag{4-11}$$

where $V_{CB(\text{sat})}$ is collector-base saturation voltage. The value of $V_{CB(\text{sat})}$ in the above expression is small and can be neglected, to give

$$I_{C(\max)} \approx \frac{V_{CC}}{R_L} \tag{4-12}$$

Emitter current must be of sufficient magnitude so that

$$I_{E1} \geq \frac{I_{C(\max)}}{\alpha_N} \tag{4-13}$$

where I_{E1} is the forward emitter current. The value of emitter current in the circuit is

$$I_{E1} = \frac{V_1 - V_{BE(\text{ON})}}{R_E} \tag{4-14}$$

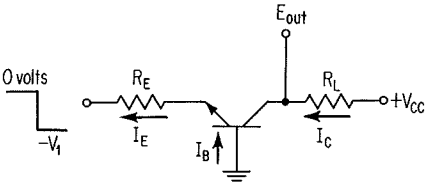

Fig. 4-8. Common-base switch.

Equations (4-12) to (4-14) allow a value of R_E to be calculated which will cause transistor saturation.

Design examples of common-emitter switching circuits are given in Sec. 6-12. The design considerations can be used with the results of the discussion above for proper design of the circuits of Figs. 4-6 and 4-8.

4-4. POWER DISSIPATION

The two operating conditions of saturation and cutoff are considered to be the two stable states of the transistor switches discussed in the preceding section. When the transistor is in saturation, a fairly large collector current may be flowing into the device. However, the collector-emitter voltage drop is small, and power dissipated in the transistor is low. A transistor at cutoff has a relatively large collector-emitter voltage, but the small value of collector leakage current causes only a small amount of power dissipation in the transistor.

It is important that the change between stable states be made quickly, as a region of high device dissipation exists between these two states. For instance, if the transistor is biased so that the quiescent operating point is at E of Fig. 4-4, the collector-emitter voltage has the value V_{CE} as shown, and the steady-state power dissipated in the transistor is fairly large as compared to the power dissipated at operating points C or D. As the operating point of a transistor makes the transition between C and D, the instantaneous device dissipation rises from a low value to a maximum and then becomes low again. Two typical plots of transistor power dissipation versus time are given in Fig. 4-9 for a grounded-emitter switching circuit implemented with two different transistors, one of which traverses the active region (region II) more quickly than the other. The two transistors have identical saturation-voltage drops and collector cutoff leakage currents. The plots of curves A and B give instantaneous power dissipation for the "fast" and "slow" transistors, respectively, and show that less average power is dissipated during the switching transition of the faster device.

The rated continuous dissipation of each device is also shown in Fig. 4-9. This level of power dissipation can be exceeded by the instantaneous power dissipation in the transistor, provided that the average transistor dissipation, over a complete cycle of operation, is below the rated maximum value.*

*This is not to be construed as meaning that abnormally large currents can be safely pulsed through a transistor even though the average power dissipation is less than the rated value. A large current can cause local heating, which may destroy the device.

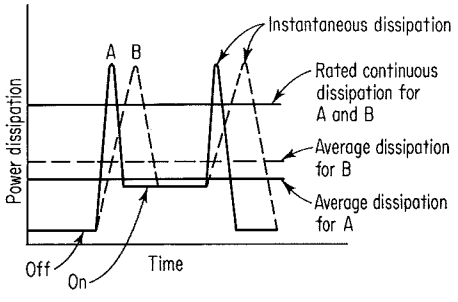

Fig. 4-9. Plots of power dissipation in fast- and slow-switching transistors.

4-5. SWITCHING-TIME TERMINOLOGY

The transition time between stable states is not only important from considerations of power dissipation but is also of concern with regard to the time relationship between input and output signals in a circuit containing one or more transistors. In order that switching speeds of individual transistors, or of circuits, may be discussed and compared, it is necessary that switching-time measurements be made in a standard manner.

A widely accepted standard of switching-time terminology and definitions is based upon response of a circuit to an input pulse of voltage.[1] Figure 4-10 shows the time relationship between input signal, collector current, and collector voltage for the circuit of Fig. 4-3. Four switching times are indicated and are discussed below.

A finite time elapses between application of the base input voltage and the start of collector-current flow in the transistor. The time interval between corresponding points of the rising input-voltage and output-current waveforms is considered to be the turn-on delay time of the circuit. This time is usually written t_d and is normally read "delay time" or "turn-on delay." The interval t_d is generally measured at values of input voltage and output current which correspond to 10 per cent of the respective maximum values of voltage and current. Turn-on delay is sometimes written t_{d1} to distinguish it from a second delay time associated with turnoff of a transistor switch.

The time required for collector current to increase from 10 to 90 per cent of its total change is defined to be the rise time of the circuit and is written t_r. Because the collector-current waveform in Fig. 4-10 begins at a zero level, the difference in time between the $0.1I_{C(\max)}$ and $0.9I_{C(\max)}$ levels is a measure of rise time.

The discussion of Sec. 1-5 pointed out that a charge storage effect of the base region causes a turnoff delay in a saturated transistor. For this reason, the time required for the collector-current waveform to decrease to 90 per cent of its maximum value, after the input voltage has decreased to 90 per cent of its maximum value, is often referred to as the storage time of the circuit and is written t_s. The notation t_s implies a storage effect. Because turnoff delay of certain circuits is often affected only slightly, or sometimes not at all, by charge storage, the turnoff delay is often written t_{d2}.

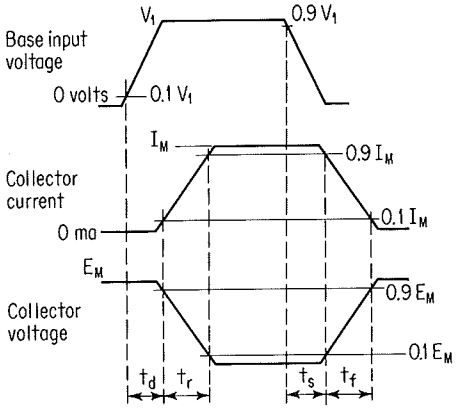

Fig. 4-10. Voltage and current waveforms for circuit of Fig. 4-3.

Fall time of the output-current waveform is the time required for this signal to fall from 90 to 10 per cent of its maximum value.

For switching times measured as described above, the turn-on time of a transistor switch is considered to be the sum of t_d (or t_{d1}) and t_r and is written t_{ON}. The turnoff time is written t_{OFF} and is the sum of t_s (or t_{d2}) and t_f.

Because voltage waveforms are normally easier to display on an oscilloscope than current waveforms are, the various switching-time measurements are usually made of the collector-voltage waveform. This technique is valid only for resistive loads in the collector circuit. For those cases where an inductor or capacitor is included as the collector load, either the collector current itself or the voltage drop across a series resistor in the collector circuit must be monitored.

4-6. FACTORS AFFECTING SWITCHING TIMES

Turn-on and turnoff times of a transistor switching circuit depend upon magnitude and waveform of the input signal, certain characteristics of the transistor itself, and the circuit configuration. A discussion is presented of factors affecting the switching response of a junction transistor in the three switching-circuit configurations discussed in Sec. 4-3. An extension of the analysis is then applied to other transistor types designed specifically for high-speed switching.

An active-region small-signal equivalent circuit of a transistor can be used to show the effect of transistor physical parameters on certain aspects of the switching-speed response of the device. Although values of the various parameters are constant over only a small operating range of collector voltage and current, the circuit configuration allows the t_d, t_r, and t_f switching times to be related to elements of the equivalent circuit.[2] A modified equivalent circuit is necessary to relate t_s to the transistor internal parameters.

t_d, t_r. Figure 4-11 is an equivalent-circuit representation of the modified-common-emitter switching circuit given in Fig. 4-6. This equivalent circuit is composed of external circuit resistances R_B and R_L and the common-base equivalent circuit of Fig. 2-5. Current out of the emitter terminal is composed of i_e and i_o. This latter component of external emitter current charges the emitter transition capacitance and is not amplified by the collector-current generator. The effect of i_o upon turn-on delay can be studied with the aid of the circuit representation of Fig. 4-12, in which the resistive and capacitive components of Fig. 4-11 are

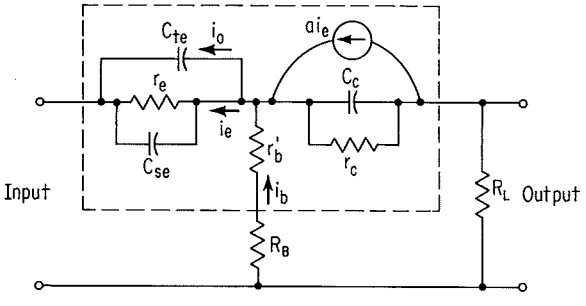

Fig. 4-11. Equivalent-circuit representation of switching circuit shown in Fig. 4-6.

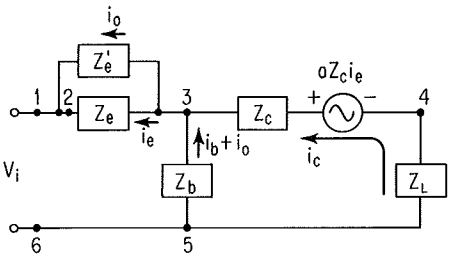

Fig. 4-12. Impedance and voltage-generator representation of network in Fig. 4-11.

represented by five impedances and the collector-current generator has been replaced by a voltage generator. Identification of the various impedance elements is given below

$$Z_e = \frac{r_e}{1 + j\omega r_e C_{se}} \qquad Z_b = r'_b + R_B$$

$$Z'_e = \frac{1}{j\omega C_c} \qquad Z_c = \frac{r_c}{1 + j\omega r_c C_c}$$

$$Z_L = R_L$$

Five circuit points are identified in Fig. 4-12 in order to describe the loops chosen for analysis. A loop voltage equation can be written for the circuit path consisting of points 123561 to obtain

$$v_i = i_e Z_e + (i_b + i_o) Z_b \tag{4-15}$$

A relationship between emitter, base, and collector current is given as

$$i_b = i_e - i_c \tag{4-16}$$

If Eq. (4-16) is substituted into Eq. (4-15), the following expression is obtained after slight rearrangement of terms:

$$v_i = i_e(Z_e + Z_b) + Z_b(i_o - i_c) \tag{4-17}$$

A loop equation can be written for the circuit path consisting of points 3453. This equation can be solved for collector current to give

$$i_c = \frac{i_e(aZ_c + Z_b) + i_o Z_b}{Z_b + Z_c + Z_L} \tag{4-18}$$

If this expression is substituted into Eq. (4-17) and the resulting expression solved for i_e, the following relationship is obtained:

$$i_e = \frac{v_i - i_o Z_b\left(1 - \dfrac{Z_b}{Z_b + Z_L + Z_c}\right)}{Z_e + Z_b\left[\dfrac{Z_c(1 - a) + Z_L}{Z_b + Z_c + Z_L}\right]} \tag{4-19}$$

Equation (4-19) shows that i_e is limited by the magnitude of i_o. This latter current, which flows to charge the emitter transition capacitance, has its maximum value at the instant a forward step of voltage is applied to the emitter terminal.

As C_{te} becomes charged, the $i_o Z_b$ term of Eq. (4-19) approaches an insignificantly small value. Since i_e is at first limited by the effect of C_{te}, the collector-current generator is initially able to amplify only a small value of i_e, and collector current is less than it would be if C_{te} were not present.

The time required to charge C_{te} is one component of the turn-on delay time and is dependent upon the OFF-state emitter-base voltage of the transistor. For a small forward- or zero-voltage bias at the emitter-base diode of an OFF transistor, the effect of C_{te} is slight. Certain considerations often make it necessary to reverse-bias the emitter-base junction of an OFF transistor. Under this operating condition, a reverse charge exists across C_{te}. A forward step of input voltage must first discharge this capacitance and then charge it, as described above. The turn-on delay is thus increased when a transistor is reverse-biased in the OFF state.

A second component of turn-on delay is caused by the finite time required for collector current to increase, irrespective of the effect of C_{te}. In order to consider the manner in which i_c increases in the modified-common-emitter circuit, independently of the shunting action of C_{te}, assume that the $i_o Z_b$ terms of Eq. (4-18) and (4-19) are negligible. In most switching circuit configurations,

$$Z_c \gg Z_L \tag{4-20}$$

and

$$Z_c \gg Z_b \tag{4-21}$$

Numerator and denominator of Eq. (4-18) can be divided by Z_c, and, to a close approximation, collector current is determined to be

$$i_c = a i_e \tag{4-22}$$

In order to obtain a simplified expression for i_e, numerator and denominator of the remaining bracketed term of Eq. (4-19) are divided by Z_c to give

$$\frac{(1 - a) + Z_L/Z_c}{Z_b/Z_c + Z_c/Z_c + Z_L/Z_c} \approx 1 - a$$

and an accurate expression for emitter current can be written

$$i_e = \frac{v_i}{Z_e + Z_b(1 - a)} \tag{4-23}$$

This equation can be substituted into Eq. (4-22) to give

$$i_c = \frac{a v_i}{Z_e + Z_b(1 - a)} \tag{4-24}$$

Parameter a in the above expression can be replaced with its frequency-dependent approximation given in Eq. (2-22). Also, impedances Z_e and Z_b can be written in terms of resistances and capacitances to give

$$i_c = \frac{a_o}{1 + j\dfrac{\omega}{\omega_a}} \frac{v_i}{\dfrac{r_e}{1 + j\omega r_e C_{se}} + (r_b' + R_B)\left(1 - \dfrac{a_o}{1 + j\omega/\omega_a}\right)} \tag{4-25}$$

The manner in which i_c varies for application of a positive-voltage step to the

circuit of Fig. 4-6 is determined by taking the Laplace transform of the above expression; this gives

$$I_c(p) = \frac{a_o}{p\left(1 + \frac{p}{\omega_a}\right)} \frac{V}{\frac{r_e}{1 + pr_eC_{se}} + (r_b' + R_B)\left(1 - \frac{a_o}{1 + p/\omega_a}\right)} \tag{4-26}$$

where V = applied voltage
p = Laplace transform variable
An expression for r_eC_{se} is given approximately as[3]

$$r_eC_{se} = \frac{1}{\omega_a} \tag{4-27}$$

If this expression is substituted into Eq. (4-26), the following result can be obtained after some rearrangement

$$I_c(p) = \frac{a_o\omega_a V}{p(r_b' + R_B)} \frac{1}{p - \omega_a[1 + r_e/(r_b' + R_B) - a_o]} \tag{4-28}$$

The inverse Laplace transform of the above expression can readily be determined and gives for collector current

$$i_c = A(1 - e^{-tB}) \tag{4-29}$$

where

$$A = \frac{a_oV}{r_e + (r_b' + R_B)(1 - a_o)}$$

$$B = \omega_a\left(1 + \frac{r_e}{r_b' + R_B} - a_o\right)$$

The manner in which the instantaneous value of i_c varies as a function of time is given by Eq. (4-29). If collector current is not limited by the external collector circuit, the final value of collector current is determined from this equation to be

$$I_C = \frac{a_oV}{r_e + (r_b' + R_B)(1 - a_o)} \tag{4-30}$$

This is a dc current and is identical to that given in Eq. (1-10) as the product of α_N and I_E.* However, since I_{B1} is readily determined for the present circuit, Eq. (4-29) can be written

$$i_c = \beta_N I_{B1}(1 - e^{-tB}) \tag{4-31}$$

Figure 4-13 shows typical plots of Eq. (4-31) for two values of base current. The collector-circuit time constant is numerically equal to $1/B$ and is the time at which each waveform has increased to 63 per cent of its final value. This figure shows that as I_{B1} is increased, the collector-current waveform reaches a particular level in less time.

Collector current in the modified-common-emitter circuit of Fig. 4-6 is limited by V_{CC} and R_L to a value less than β_N times the dc base current. However, applica-

* Collector leakage current is neglected in the present discussion.

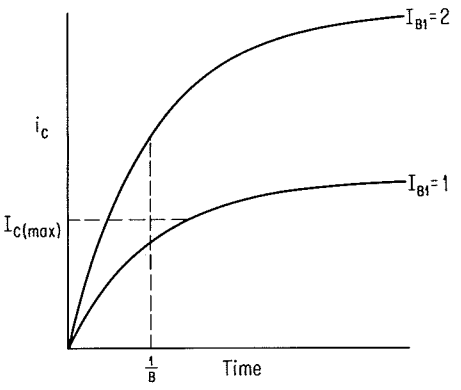

Fig. 4-13. Typical plots of Eq. (4-31) for two values of base current.

tion of a forward-bias emitter-base voltage causes the rising collector waveform to follow a path given by Eq. (4-31) until the transistor saturates and collector current is clamped to $I_{C(\max)}$. This clamped level of collector current is shown in Fig. 4-13. For a fixed value of $I_{C(\max)}$, the $0.1I_{C(\max)}$ point of the rising collector-current waveform (which is a measure of turn-on delay) is reached in less time for the larger of the two base currents shown.

If only enough base current is present barely to saturate the transistor, the second component of turn-on delay will have its maximum value. As base current increases beyond the value required for saturation, the transistor is considered to be overdriven. An overdrive factor is written

$$\text{Overdrive factor} = \frac{\beta_N I_{B1}}{I_{C(\max)}} \tag{4-32}$$

It is clear that an increase in overdrive factor reduces this component of turn-on delay.

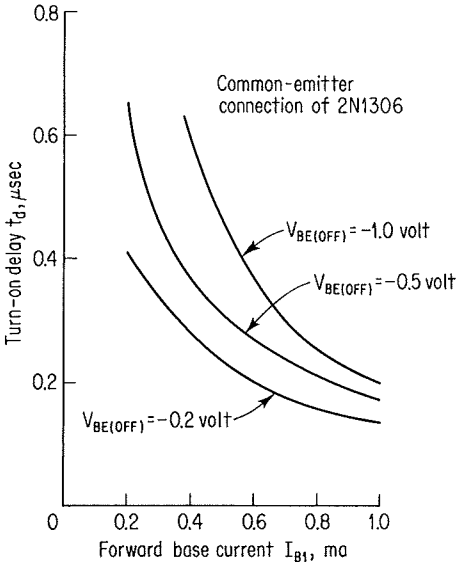

Fig. 4-14. Effect of I_{B1} and $V_{BE(OFF)}$ on turn-on delay.

A 2N1306 germanium-alloy transistor is connected as a common-emitter switch.* Measured plots of turn-on delay versus forward base current, for various values of reverse-bias base-emitter voltage, are shown in Fig. 4-14. These curves show that turn-on delay decreases for an increase in forward base current and increases for larger reverse-bias base-emitter voltages.

Rise time of a switching circuit has previously been defined as the interval of time between the 10 and 90 per cent points of the total change in the increasing collector-current waveform. The time difference between these current levels for the circuit of Fig. 4-6 can be determined analytically from Eq. (4-31). A graphical solution for t_r can be obtained by measuring the time interval between the $0.1I_{C(\max)}$ and $0.9I_{C(\max)}$ points of the plotted collector-current waveform. Figure 4-13 shows that rise time is reduced as the overdrive factor is made larger.

Emitter and base currents in the circuit of Fig. 4-6 are limited to safe values by the presence of R_B. These currents can also be limited by employing an emitter resistor as shown in the grounded-base circuit of Fig. 4-8. The equivalent circuit used for an ac analysis of this circuit is the same as that given in Fig. 4-12, except that Z_e and Z_b now have different values. The impedance Z_e' contributes only to turn-on delay and is neglected in the following analysis of collector-current increase; Z_e and Z_b now have the values

$$Z_e = R_E + \frac{r_e}{1 + j\omega r_e C_{se}}$$

$$Z_b = r_b'$$

Because the equivalent-circuit configuration under consideration is identical to that used to determine collector-current increase in the modified-common-emitter circuit, an expression identical to that of Eq. (4-24) can now be derived.† If, in Eq. (4-24), present values of Z_e and Z_b are inserted, r_eC_{se} is replaced by $1/\omega_a$ [see Eq. (4-27)], and the Laplace transform is taken of the resulting expression, the transform expression for collector current can be described by

$$I_C(p) = \frac{a_o\omega_a V}{p(R_E - r_b')} \frac{1}{p + \omega_a[1 + (r_e - r_b'a_o)/(R_E + r_b')]} \tag{4-33}$$

Taking the inverse Laplace transform of the above equation yields

$$i_c = C(1 - e^{-tD}) \tag{4-34}$$

where

$$C = \frac{a_o V}{R_E + r_b'} \frac{1}{1 + (r_e - r_b'a_o)/(R_E + r_b')}$$

$$D = \omega_a\left(1 + \frac{r_e - r_b'a_o}{R_E + r_b'}\right)$$

Equation (4-34) can also be written

$$i_c = \alpha_N I_{E1}(1 - e^{-tD}) \tag{4-35}$$

* The same factors affect t_d in the common-emitter and modified-common-emitter configurations.
† Inequalities in Eqs. (4-20) and (4-21) are still valid.

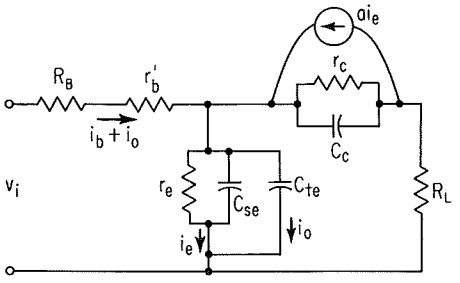

Fig. 4-15. Equivalent-circuit representation of common-emitter inverter of Fig. 4-3.

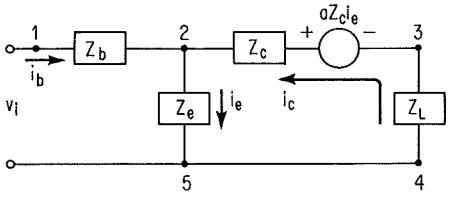

Fig. 4-16. Impedance and voltage-generator representation of network in Fig. 4-15.

Effects of transistor and circuit parameters on turn-on delay and rise time of the common-emitter inverter of Fig. 4-3 are determined with the equivalent-circuit representations of Figs. 4-15 and 4-16. The circuit of Fig. 4-15, which includes the external base resistor R_B and the common-emitter equivalent circuit of Fig. 2-17, shows that a charge must be supplied to emitter transition capacitance C_{te} before appreciable collector current can flow. The presence of C_{te} is disregarded in the equivalent-circuit configuration of Fig. 4-16, which is used to obtain an equation for collector-current increase as a function of time. The various impedance elements shown have the same identification as in Fig. 4-12.

Voltage equations can be written for the two circuit loops shown in Fig. 4-16. The following equation is obtained for loop 1251:

$$v_i = i_b(Z_b + Z_e) + i_c Z_e \tag{4-36}$$

The second loop consists of points 23452 and contains i_c and i_e currents. If i_e is written in terms of i_b and i_c [see Eq. (4-16)] and this expression is substituted for i_e in the voltage equation for the second loop, collector current can be described by

$$i_c = \frac{i_b(aZ_c - Z_e)}{Z_e + Z_L + Z_c(1 - a)} \tag{4-37}$$

If the above equation for i_c is substituted into Eq. (4-36), base current is determined to be

$$i_b = \frac{v_i}{Z_b + Z_e + [(aZ_c - Z_e)Z_e]/[Z_e + Z_L + Z_c(1 - a)]} \tag{4-38}$$

The following relationships exist in most switching circuits

$$Z_c(1 - a) \gg Z_e^2 \tag{4-39}$$

$$Z_c(1 - a) \gg Z_L \tag{4-40}$$

and allow collector current and base current to be written

$$i_c = \frac{i_b a}{1 - a} \tag{4-41}$$

$$i_b = \frac{v_i}{Z_b + Z_e/(1 - a)} \tag{4-42}$$

The expression for base current given in Eq. (4-42) can be substituted into Eq. (4-41) to give

$$i_c = \frac{av_i}{Z_e + Z_b(1 - a)} \tag{4-43}$$

Equation (4-43) is identical to Eq. (4-24). Thus, expressions for increasing collector current in the common-emitter circuit of Fig. 4-3 are given by Eqs. (4-29) and (4-31).

Collector-current increase was measured for the 2N1306 germanium-alloy transistor in the common-emitter and modified-common-emitter switching circuits. The two circuits had identical values of external base resistance, collector load resistance, and magnitude of input voltage (but of opposite polarity). These measured plots are shown in Fig. 4-17, together with the two circuit configurations. Maximum collector current in the common-emitter circuit is given by

$$I_{C(\max)} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_L} \tag{4-6}$$

In order to test both circuits at the same level of saturated collector current, the V_{CC} supply was grounded for the modified-common-emitter circuit; maximum collector current for this circuit is determined from Eq. (4-10) to be

$$I_{C(\max)} = \frac{V_1 - V_{CE(\text{sat})}}{R_L} \tag{4-44}$$

Substitution of the actual circuit voltages into the above two expressions shows that the collector current is approximately 20 ma for each circuit.

Figure 4-17 shows an unexpected difference between collector current in the two circuits. Collector-emitter capacitance of the transistor causes a negative step of voltage to appear at the collector terminal of the modified-common-emitter

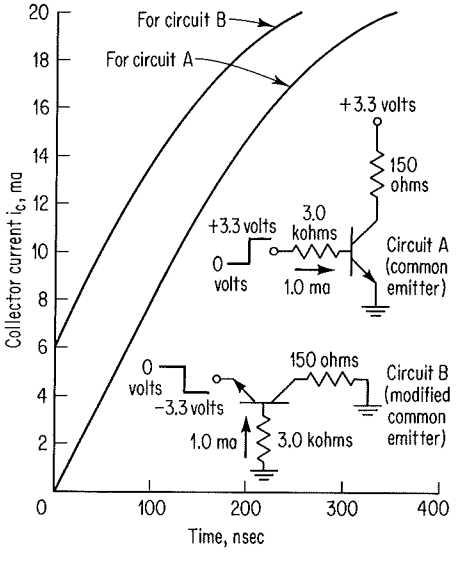

Fig. 4-17. Measured plots of collector-current increase for the depicted circuits.

circuit when the input signal is applied. This negative-voltage level at the collector causes an initial increase in collector current which is not considered in the previous discussion. Except for a constant offset between the two measured curves, the current waveforms of the two circuits increase in exactly the same manner.

The analysis thus far of collector-current increase in the modified-common-emitter, common-base, and common-emitter circuits has been for a step of applied input voltage. Rise time of the common-emitter and modified-common-emitter circuits is increased if a step of input current, rather than a step of input voltage, is applied to the stage. For the modified-common-emitter circuit of Fig. 4-6, an approximate expression for collector current is given by Eq. (4-22). With the relationship given in Eq. (4-16), the following expression can be obtained from Eq. (4-22):

$$i_c = \frac{ai_b}{1 - a} \tag{4-45}$$

Base current is now considered to be the input current to the circuit of Fig. 4-6, and the switching-circuit configuration can be changed to the common-emitter circuit of Fig. 4-3.* Substitution of the frequency-dependent expression for a into Eq. (4-45) allows collector current to be written

$$i_c = \frac{a_o i_b}{(1 - a_o) + j\omega/\omega_a} \tag{4-46}$$

If a step of forward base current is assumed for the grounded-emitter circuit, the time-dependent expression for collector current is determined to be

$$i_c = \beta_N I_{B1}(1 - e^{-t(1-a_o)\omega_a}) \tag{4-47}$$

where β_N has been substituted for $a_o/(1 - a_o)$.

Equations (4-31) and (4-47) are two time-dependent expressions for collector current in both the modified-common-emitter and common-emitter circuits. The first of these equations is an expression for collector-current increase for a step of applied base voltage, and the second expression gives collector-current increase for a step of input current to the base. The two equations are identical except for the time-independent exponential multiplier, the reciprocal of which is the time constant of the expression. The time constant for Eq. (4-31) is

$$T_V = \frac{1}{B} = \frac{1}{\omega_a[1 + r_e/(r_b' + R_B) - a_o]} \tag{4-48}$$

where T_V is the time constant for a step of input voltage, and the time constant for Eq. (4-47) is

$$T_I = \frac{1}{\omega_a(1 - a_o)} \tag{4-49}$$

where T_I is the time constant for a step of input current. If external base resistance R_B in the circuit of Fig. 4-3 or 4-6 is made infinitely large, the time-constant

* Equation (4-45) can be obtained from Eq. (4-37) by dividing numerator and denominator by Z_c and making use of inequalities in Eqs. (4-39) and (4-40).

expression of Eq. (4-48) becomes that of Eq. (4-49). An infinite input impedance (R_B in this case) implies a current drive, and one would expect to obtain the time constant for a step of input current.

In actual common-emitter or modified-common-emitter switching circuits, the input signal is not strictly a step of base voltage or a step of base current. The value of series resistor in the base circuit determines whether the input signal approaches a current step or a voltage step. For a typical range of external base resistance, there is little effect upon rise time for wide variation in the value of resistor used, provided that the value of I_{B1} is adjusted to the same magnitude for each resistance value. This is illustrated in Fig. 4-18, which shows measured plots of increasing collector current versus time for three different values of external base resistance in the common-emitter connection of a 2N1306 transistor. The value of I_{B1} is equal to 1 ma for each plot. Collector current rises fastest for the lowest value of R_B. However, as R_B is increased from 200 ohms to 2.2 kilohms, there is only a slight falloff in collector-current increase. No measurable difference exists between the plots for R_B equal to 2.2 kilohms and R_B equal to 4.7 kilohms.

Equation (4-22) can be used to determine collector-current increase for a step of emitter current to the common-base circuit. The Laplace transform of this equation for a step of i_e is

$$I_C(p) = \frac{\omega_a a I_e}{p(p + \omega_a)} \tag{4-50}$$

The inverse Laplace transform of this expression yields*

$$i_c = \alpha_N I_{E1}(1 - e^{-t\omega_a}) \tag{4-51}$$

* Equation (4-51) can be obtained by making R_E infinitely large in Eq. (4-35).

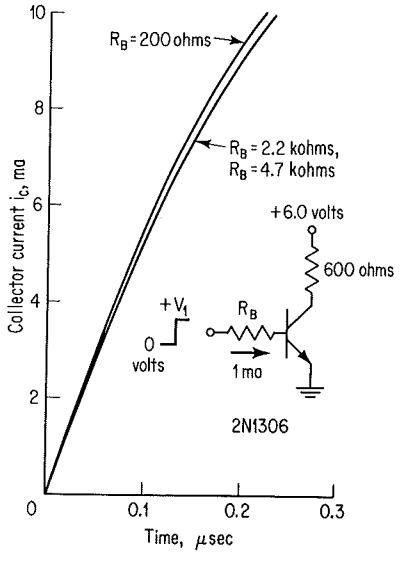

Fig. 4-18. Measured curves showing effect of R_B on collector-current increase.

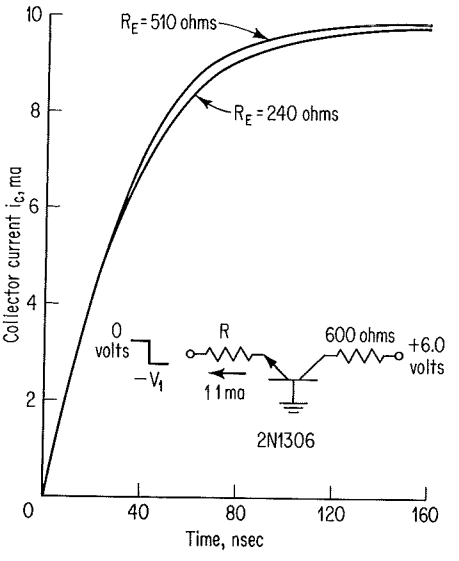

Fig. 4-19. Measured curves showing effect of R_E on collector-current increase.

A comparison of Eq. (4-51) with Eq. (4-35) shows that the circuit time constant is different for a step of emitter current than for a step of emitter voltage. Relative magnitudes of r_e and r'_b determine which of the above time constants is smaller. Plots of collector-current increase versus time are given in Fig. 4-19 for two typical values of R_E and constant values of I_{E1} in the common-base connection of a 2N1306 transistor. These curves show that the value of R_E has only a slight effect upon collector-current increase.

In order to illustrate the validity of Eqs. (4-31) and (4-47) for the common-emitter configuration, a measured curve of collector current versus time is plotted for an actual switching circuit and compared with the curves determined by the two equations. The three curves, together with the switching-circuit configuration, are shown in Fig. 4-20. (An additional calculated curve for $C_c = 5$ pf is shown and is discussed later.) The circuit diagram shows that base turn-on current to the 2N1306 transistor is approximately 1 ma and that collector current is limited to slightly less than 20 ma. Values of β_N and ω_a used in the calculations correspond to actual measurements made on the transistor. Because the above two parameters are not constant throughout the switching region, they were measured at an operating point which lies approximately halfway between the saturated and cutoff conditions. The values thus obtained are considered to be

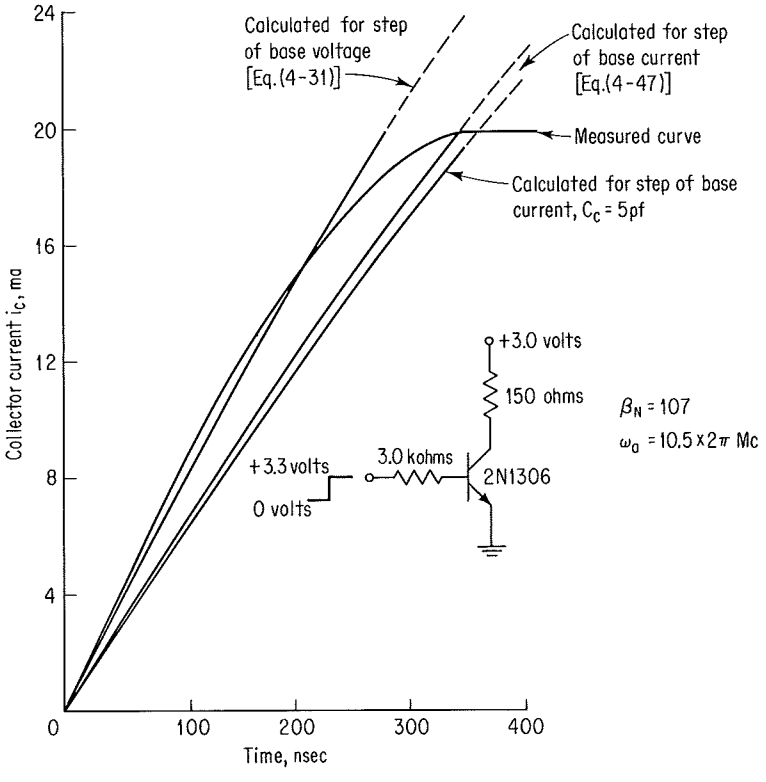

Fig. 4-20. Measured and calculated curves of collector-current increase.

average values and are used as constant values in the calculations. Values of β_N and ω_a were determined at an I_C of 10 ma and a V_{CE} of 1.5 volts. The value of a_o is calculated from the relationship

$$a_o \approx \alpha_N = \frac{\beta_N}{\beta_N + 1} \tag{4-52}$$

For a maximum current of 20 ma, an average value of 2.6 ohms is selected for r_e. The value of 50 ohms for r'_b is approximately correct.

The two curves calculated from Eqs. (4-31) and (4-47) differ from each other but are roughly similar to the measured plot of collector-current increase and show that the above equations are useful for an approximate determination of collector-current response to an input signal.

A more detailed treatment of collector-circuit transient response would include the effect of internal collector capacitance C_c. This analysis has been presented in the literature and shows that for the common-emitter configuration, the exponential term in Eq. (4-47) becomes

$$\frac{-t(1 - a_o)\omega_a}{1 + \omega_a R_L C_c}$$

for an input step of base current.[4] The effect of C_c is illustrated in the plot of Fig. 4-20, which shows the calculated increase of collector current for an assumed C_c of 5 pf. Equation (4-47), modified with the term given above, is used for this calculation. The effect of internal collector capacitance is to increase rise time of the circuit. Larger values of R_L also increase rise time.

Equations (4-35) and (4-51) show that regardless of whether the input signal to a common-base stage is considered to be a voltage step or a current step, collector-current magnitude at any instant of time is directly proportional to the value of α_N (or a_o).* However, the effect of a_o upon collector-current increase in the common-emitter configuration is not immediately clear. Equations (4-31) and (4-47) show that, for an increase in a_o (which increases the magnitude of β_N), there is a simultaneous decrease of the term within the exponential portion of each equation. Because the effect of a_o is similar in Eqs. (4-31) and (4-47), only Eq. (4-47) will be considered. Constant values of I_{B1}, t, and ω_a will be assumed in order to determine the effect of a_o upon collector current.

As a numerical example of the effect of a_o upon collector-current increase of the common-emitter stage, consider that $t\omega_a = 6.6$, $I_{B1} = 1$ ma, and that a_o has values ranging from 0.960 to 1.000. Equation (4-47) can now be written

$$i_c = \frac{a_o}{1 - a_o}(1 - e^{-6.6(1-a_o)}) \tag{4-53}$$

This equation is useful for values of a_o less than 1. For a_o equal to 1, the value of i_c becomes the product of infinity times zero, which is clearly indeterminate. L'Hospital's rule is used to determine the limit of the above equation as $a_o \rightarrow 1$. This limit does exist and is equal to 6.60 for the present numerical example.

* The parameters α_N and a_o are considered to have the same magnitude.

Table 4-1. Values of i_c Calculated from Eq. (4-53)

a_o	i_c
0.960	5.55
0.970	5.80
0.980	6.02
0.990	6.33
0.996	6.47
0.998	6.54
1.000	6.60

Table 4-1 gives calculated values of i_c for various values of a_o and shows that, for constant values of t, I_{B1}, and ω_a, i_c becomes larger as a_o increases in magnitude.

Turn-on delay and rise time are affected by external load capacitance C_L. Figures 4-21 and 4-22, respectively, give measured plots of t_d and t_r versus C_L for a common-emitter connection of the 2N1306 transistor. These figures show that both t_d and t_r increase as C_L is made larger.

t_s. The discussion of Sec. 1-5 indicated that saturation of a transistor occurs when the collector-base junction becomes forward-biased and that a further increase in base current causes an excess charge to accumulate in the base region. If the forward-bias base-emitter voltage is suddenly removed, the excess base charge flows into the collector, and the collector-base junction remains forward-biased until the minority-carrier gradient in the base region reaches zero at the collector junction. At the instant of time of zero gradient at the collector-base junction, the collector no longer emits carriers into the base region, and the transistor comes out of saturation.

A positive base-emitter voltage exists (for the N-P-N transistor) as long as there is a potential gradient in the base region.[5,*] An excess base charge causes this voltage to have the magnitude of $V_{BE(ON)}$. Consider the switching circuit of Fig. 4-23, in which the applied voltage V_1 causes saturation of the transistor. If switch S_1 is opened, the base-emitter diode is open-circuited, and excess base charge flows into the collector.†

Instead of opening S_1 to remove the forward-bias voltage, switch S_2 can be closed to ground point A. This places R_B across the base-emitter diode of the transistor, and a portion of the stored base charge is now able to flow through R_B into ground. A third method of turning the transistor off is to keep S_1 closed,

* Reference 5 analyzes the transient response of a P-N junction and shows that a forward-biased junction remains forward-biased for a finite time after removal of the external-bias voltage.

† A portion of the base charge may recombine in the base region.

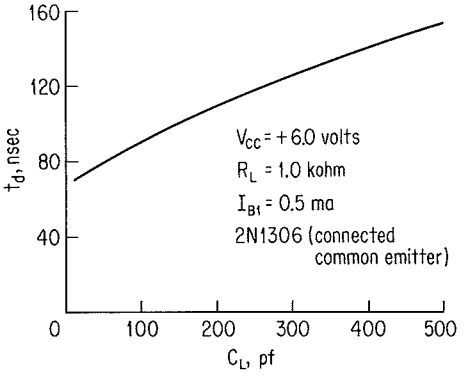

Fig. 4-21. Measured curve showing effect of load capacitance on turn-on delay.

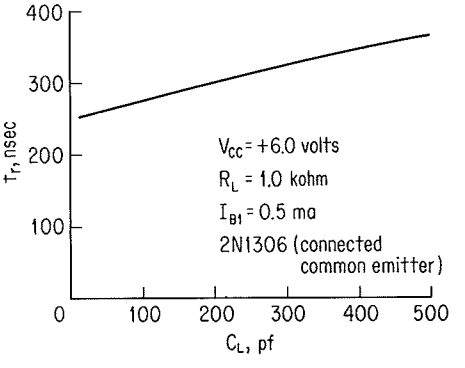

Fig. 4-22. Measured curve showing effect of load capacitance on rise time.

let S_2 remain open, and close switch S_3. This applies reverse voltage V_2 to point A and causes charge to be removed more quickly from the base.

Reverse base-drive current is referred to as I_{B2} in order to distinguish it from I_{B1}, the forward base-drive current. With S_1 closed, current flow out of the base for the circuit of Fig. 4-23 is written

$$I_{B2} = \frac{V_{BE(ON)}}{R_B} \tag{4-54}$$

for closure of S_2 and is given as

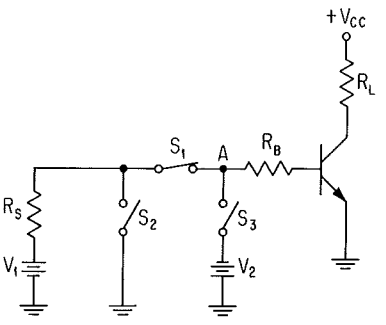

Fig. 4-23. Various turnoff methods for inverter circuit.

$$I_{B2} = \frac{V_2 + V_{BE(ON)}}{R_B} \tag{4-55}$$

for closure of S_3 only. Each of the above expressions for I_{B2} indicates an instantaneous maximum value of base current which flows because of a minority-carrier charge in the base region. As this charge decreases in magnitude, the value of reverse base current diminishes to a small reverse-leakage current. Figure 4-24 shows a typical plot of forward and reverse base current in a transistor switch. The base-emitter diode is switched from forward to reverse conduction at time t_1.

Several papers have analyzed the storage time of transistor switches in the common-emitter configuration.[2,6,7] The resulting storage-time equations include the forward- and reverse-bias currents and show that storage time increases as I_{B1} is increased and decreases as I_{B2} is increased. Figure 4-25 shows measured curves of storage time versus reverse base drive for constant I_C and constant I_{B1}.

Reverse drive current to the common-base circuit is obtained by a sudden reversal of the forward drive voltage at the input terminal. This causes an instantaneous reverse emitter current I_{E2} to remove charge from the base region. Moll[2] shows that for the common-base connection, storage time increases for larger I_{E1} and decreases for larger I_{E2}.

t_f. Fall time of a transistor switch can be determined with the same equivalent circuit used in a study of the rise time. However, in order to understand the manner in which collector current decays, for a sudden decrease of input drive current, a close examination must be made of the current generator in the collector branch of the equivalent circuit.

For the equivalent circuit of Fig. 4-12, Eq. (4-22) gives an approximate expression for collector current in terms of complex current gain and emitter current and shows that i_c is the product of a and i_e. One might infer from this equation that a sudden decrease of i_e to a zero level would immediately cause i_c also to decrease to zero. This conclusion is not valid, however. The previous discussion of storage time indicated that although emitter current ceases to flow, collector

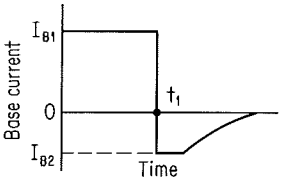

Fig. 4-24. Forward and reverse base-current flow in transistor switch.

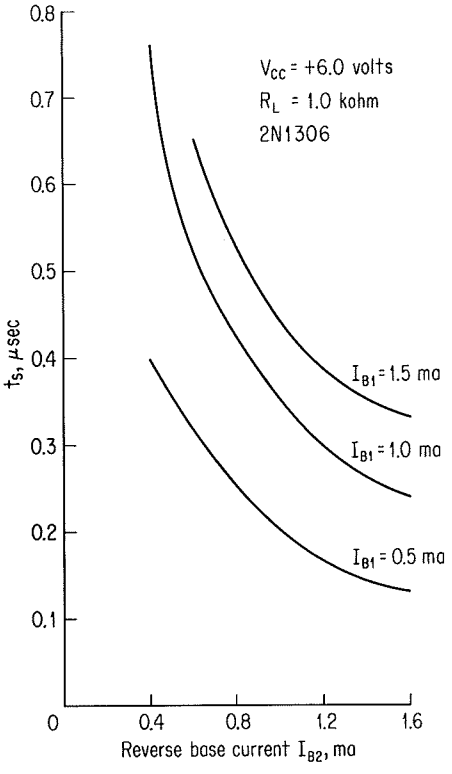

Fig. 4-25. Measured curves showing effect of forward and reverse base current on storage time.

current remains at its saturated value for the finite time required for the minority-carrier density gradient in the base region to become zero at the collector junction. This density gradient at the edge of saturation is shown in Fig. 4-26 as curve *A*. Because emitter current is no longer flowing in the circuit under discussion, minority carriers are not injected from the emitter into the base region, and the density gradient in the base region must eventually reach zero at the emitter junction. Curve *B* of Fig. 4-26 shows this condition of zero gradient at both the collector and emitter junctions. A decaying collector current flows during the change in gradient from curve *A* to curve *B*.

Mathematically, the collector-current generator in the transistor equivalent circuit is analogous to a series *RL* circuit.[1] The discussion of Sec. 2-2 showed that the base transport factor causes the output of the collector-current generator to decrease at higher frequencies. The frequency variation of a was given in Fig. 2-10 and is shown again in Fig. 4-27. This frequency variation of current gain is similar to the current response (for a sine-wave input) of the series *RL* circuit of Fig. 4-28. Values can be selected for *R* and *L* to cause the current response curve of this *RL* circuit to correspond exactly to the curve of Fig. 4-27.

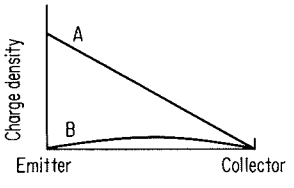

Fig. 4-26. Density gradient in base region; edge of saturation *A*, collector-current cutoff *B*.

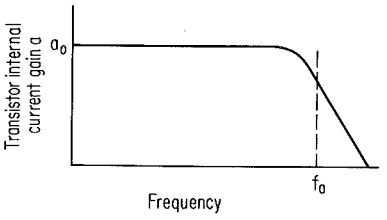

Fig. 4-27. Frequency variation of transistor internal-current gain.

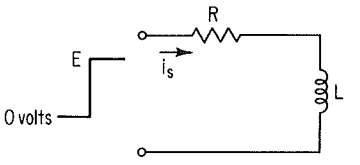

Fig. 4-28. *RL* equivalent circuit for collector-current generator.

The current-transfer equation of the series *RL* circuit can be written

$$i_s = \frac{e}{R}\frac{1}{1 + j\omega L/R} \tag{4-56}$$

where i_s = instantaneous value of current
e = instantaneous value of applied voltage

The form of this expression is identical to that of Eq. (4-46), which relates to collector current in either the modified-common-emitter circuit of Fig. 4-6 or the common-emitter circuit of Fig. 4-3. Application of a voltage step to the *RL* circuit causes a current flow through R and L which varies according to the relation

$$i_s = \frac{E}{R}(1 - e^{-tR/L}) \tag{4-57}$$

where E is the magnitude of the voltage step. The positive direction of flow for i_s is given in Fig. 4-28.

A sudden decrease of applied voltage to zero magnitude in the *RL* circuit would not cause i_s suddenly to become zero. Rather, the current decreases exponentially from the maximum value it has reached (I_S) to zero. An expression for this decaying current is

$$i_s = I_S e^{-tR/L} \tag{4-58}$$

Because Eqs. (4-46) and (4-56) are of the same form, an expression for the decay of generated current in the transistor circuits of Figs. 4-6 and 4-3, for a sudden decrease to zero of base current, must be similar to Eq. (4-58) and is written*

$$i_c = I_{C1}(e^{-t(1-\alpha_0)\omega_\alpha}) \tag{4-59}$$

where I_{C1} is the collector-current magnitude at the instant that base current becomes zero. A typical

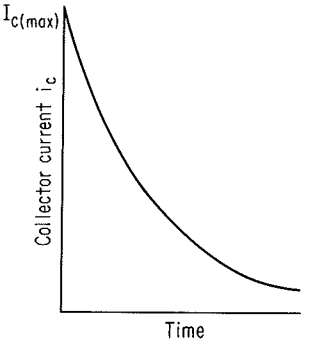

Fig. 4-29. Typical plot of Eq. (4-59).

* Equation (4-46) is not valid when the transistor is in the saturation region (region III). However, transistor operation is in region II during the fall-time period, and the equation does apply. Equation (4-59) is thus an expression for collector current after the transistor has come out of saturation.

plot of Eq. (4-59) is given in Fig. 4-29. The current is assumed to have risen to $I_{C(\max)}$. Fall time can be determined from a plot of this type.

The preceding discussion of fall time has shown that both from a consideration of the minority-carrier density gradient in the base region and from a mathematical consideration, a finite time is required for collector current to decrease to zero after removal of the input signal.

A reverse turnoff current to the transistor has considerable effect upon fall time of the output waveform. It was mentioned in Sec. 2-2 that the current generator in the collector branch of the equivalent circuit amplifies both forward and reverse emitter currents. If collector current were able to flow in the circuit of Fig. 4-6 (or Fig. 4-3), and if this current were not limited by the external collector circuit, the collector-current magnitude would eventually become

$$I_C' = \beta_N I_{B2} \tag{4-60}$$

where I_C' is the maximum reverse collector current. Although this reverse collector current cannot flow, the forward collector current flowing at the instant of turnoff falls toward this reverse-current magnitude.

Collector-current decay for a reverse base current can be analyzed by study of the analogous *RL* series circuit representation of the collector-current generator. Application of a reverse step of base current to an ON transistor is analogous to applying a reverse voltage to an *RL* circuit in which a direct current is flowing. Consider that the *RL* circuit of Fig. 4-28 has the direct current I_S flowing in it and that a reverse voltage step E is suddenly applied to the input terminals. This reverse voltage opposes the flow of I_S. An expression for instantaneous current is readily determined to be

$$i_s = -\frac{E}{R} + \left(\frac{E}{R} + I_S\right)e^{-tR/L} \tag{4-61}$$

The analogous expression for generated current in the transistor switch, for a reverse step of base current, is given as*

$$i_c = -\beta_N I_{B2} + (\beta_N I_{B2} + I_{C1})e^{-t(1-\alpha_0)\omega_\alpha} \tag{4-62}$$

Figure 4-30 shows a measured plot of fall time versus I_{B2} for an inverter stage.

Collector-current decay in the common-base configuration can be determined in a manner analogous to that described above for the modified-common-emitter and common-emitter circuits. For a step reduction of I_{E1} to zero, the expression for collector current becomes

$$i_c = I_{C1}e^{-t\omega_\alpha} \tag{4-63}$$

and for a reverse step of emitter current, collector current is determined to be

$$i_c = -\alpha_N I_{E2} + (\alpha_N I_{E2} + I_{C1})e^{-t\omega_\alpha} \tag{4-64}$$

For each of the three switching-circuit configurations, fall time increases for larger values of internal collector capacitance, external load capacitance, or load resistance. Figure 4-31 shows a common-emitter circuit having a load capaci-

* This equation is valid only for $i_c \geq 0$.

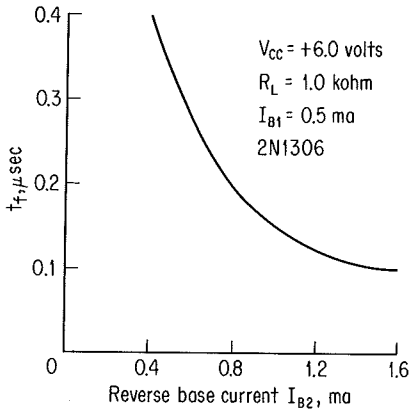

Fig. 4-30. Measured curve showing effect of reverse base current on fall time.

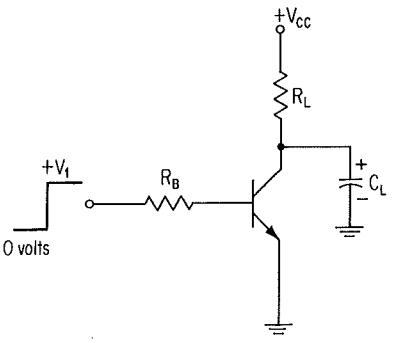

Fig. 4-31. Inverter stage with external-load capacitance.

tance of C_L. Consider that the transistor has remained at cutoff sufficiently long for the capacitor to charge to approximately the supply-voltage magnitude. The figure shows voltage polarity across the capacitor. When the transistor is driven into saturation, the capacitor is discharged through the low-impedance (usually less than 50 ohms) collector-emitter path of the transistor. Regardless of how quickly the transistor may be switched back to the cutoff state, the load capacitor must charge through resistance R_L, and the charging-voltage (or current) curve of the capacitor can be no better than that determined by the R_LC_L product. Stray circuit capacitance at the collector terminal, or discrete external circuit capacitance, dictates that the value of R_L must be small if a short fall time is required.

4-7. HIGH-SPEED SWITCHING TRANSISTORS

The diffused-base transistor (described in Sec. 3-3) has certain characteristics which make it superior to the junction transistor as a high-speed switching element.* Minority carriers are accelerated through the diffused-base region, whereas carriers injected into the base of a junction transistor simply drift across the base region. Acceleration of carriers through the base region causes the diffused-base unit to turn on more quickly than the junction device. The diffused-base transistor is, in general, physically smaller than the junction device and consequently has an improved transient response. Saturation effects are minimized in the diffused-base transistor, and storage time is usually reduced from that of the junction transistor. The epitaxial diffused-base transistor, because of its lower internal collector capacitance and low collector-region storage, is capable of even faster switching speeds than can be obtained with either the junction transistor or the nonepitaxial diffused-base transistors.

Measured plots of t_d, t_r, t_s, and t_f are given in Fig. 4-32*a* to *d* for an alloy-junction

* The term junction transistor refers to the nondiffused grown-junction or alloy-junction device.

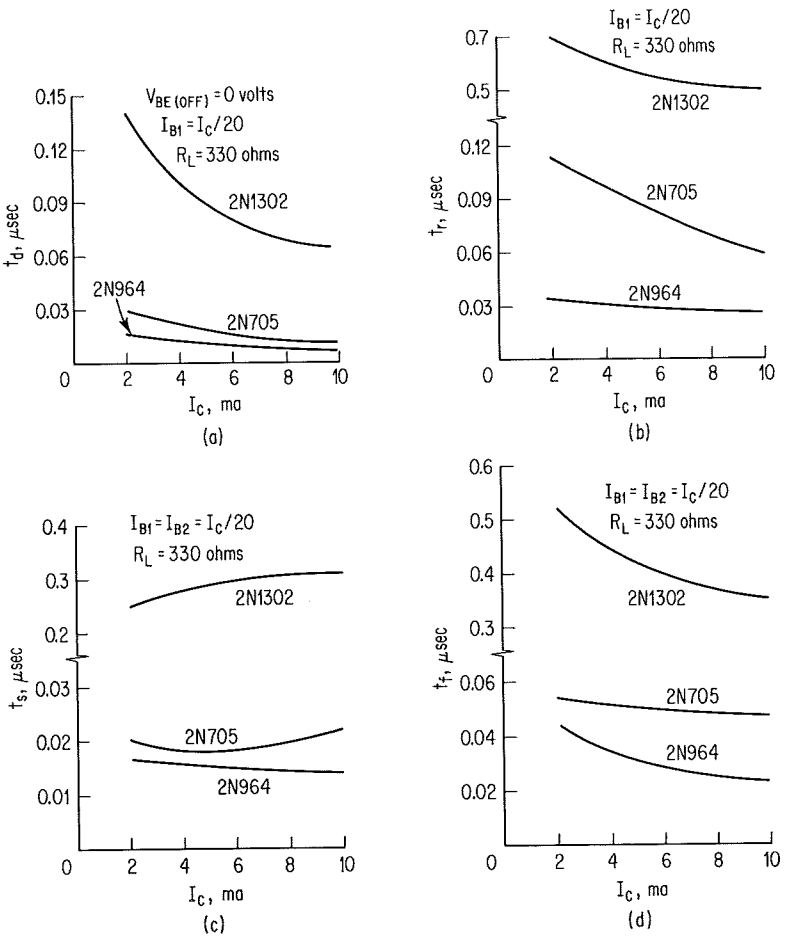

Fig. 4-32. Switching-speed plots for three transistor types.

transistor (2N1302), a diffused-base mesa transistor (2N705), and an epitaxial diffused-base mesa transistor (2N964). The figure shows that switching speed of the nonepitaxial diffused-base transistor is improved over that of the alloy-junction device. The epitaxial transistor affords an even greater reduction of total switching time.

4-8. COMPARISON OF SWITCHING-CIRCUIT CONFIGURATIONS

Various switching-circuit applications impose different requirements on circuit operating characteristics. In general, one or more of the following circuit considerations is of importance in a switching-circuit application:

1. Dc voltage gain.
2. Dc current gain.
3. Switching response.

This section compares the common-base, modified-common-emitter, and common-emitter circuits with respect to each of the above circuit characteristics. Transistor operation is from cutoff to saturation; voltage and current levels are steady-state values. Transistor leakage currents are neglected in this discussion.

DC Voltage Gain. Figure 4-33 shows the three switching-circuit configurations to be discussed and indicates a four-terminal network representation of each circuit. Input voltage to each of the above networks is the actual value of voltage appearing across the input terminals. For a zero-level input signal, voltage across the output terminals of each network is very nearly equal to V_{CC}. If voltage gain were defined to be the ratio of output-voltage magnitude to input-voltage magnitude, the gain would be infinite for a zero-level input signal. The important consideration in these circuits is the change in output-voltage level for a change in input-voltage level. Thus, the ratio of voltage developed across R_L to the actual input-voltage magnitude is defined to be the voltage gain of these switching circuits.

Collector voltage of the common-base switch can become only slightly negative with respect to the base, which is at ground potential. Hence, the voltage drop across R_L is approximately equal to the collector supply voltage, and voltage gain of the common-base configuration can be written

$$A_V \approx \frac{V_{CC}}{V_1} \tag{4-65}$$

where A_V = voltage gain
V_1 = input-signal magnitude

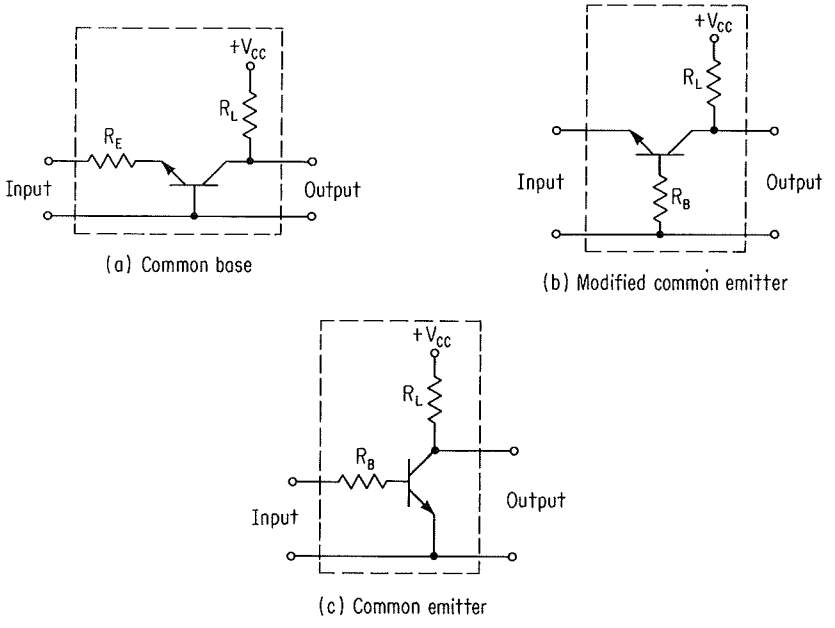

Fig. 4-33. Four-terminal network representation of three switching-circuit configurations.

This voltage gain can be greater or less than unity.

The modified-common-emitter switch has a saturated collector potential which differs from the emitter input voltage by $V_{CE(sat)}$. If this small saturation-voltage drop is neglected, total voltage drop across R_L is equal to the numerical sum of V_{CC} and V_1; voltage gain becomes

$$A_V \approx \frac{V_{CC} + V_1}{V_1} = 1 + \frac{V_{CC}}{V_1} \tag{4-66}$$

Voltage gain of this circuit is seen to be always greater than unity.

Voltage drop across R_L in the common-emitter circuit is approximately equal to the magnitude of V_{CC}, and voltage gain of this circuit is given by Eq. (4-65).

DC Current Gain. In order for a transistor to function, an input-current flow is required. This current must be supplied by the input-signal voltage acting through the input impedance. Input current to a transistor switching circuit controls current at the output terminal of the transistor. Current gain for each of the circuits in Fig. 4-33 is defined to be the ratio of collector-current magnitude to input-current magnitude. This current gain is not to be confused with the transistor parameters α_N or β_N. These latter current gains are determined solely by the transistor and are always a ratio of collector current to input current when there is no external circuit to limit collector-current magnitude.

Two examples will illustrate that current gain of a switching circuit may be equal to or less than the intrinsic current gain of the transistor. The examples describe current and voltage levels in the common-base circuit shown in Fig. 4-33*a*. An important consideration is that the collector-base diode will not allow the collector terminal to become more than a few tenths of a volt negative with respect to the grounded base.

EXAMPLE 4-1

Consider that R_L has a value of 1.0 kilohm, V_{CC} is equal to 1.5 volts, and the transistor has an α_N of 0.9; an input current I_E of 0.8 ma is applied to the circuit. The values of R_L and V_{CC} indicate that approximately 1.5 ma of collector current can flow before the collector voltage falls to ground potential. The product of α_N and I_E is equal to only 0.72 ma; this magnitude of collector current would cause the collector voltage to decrease to only 0.78 volt, and transistor operation would still be in region II. Collector current is seen to be limited only by input-current magnitude and α_N of the transistor. Because the collector external circuit does not restrict collector-current magnitude, a collector current of 0.72 ma does flow, and current gain of the circuit is identical to α_N of the transistor.

EXAMPLE 4-2

Consider that all conditions remain the same as for Example 4-1, except that R_L is now increased to 3.0 kilohms. The maximum allowable output current is now approximately 0.5 ma. For an input current of 0.8 ma, current gain of the circuit becomes 0.5/0.8, or 0.625. This circuit current gain, which is seen to be considerably smaller than α_N of the transistor, is sometimes referred to as a "forced current gain."

Expressions are presented below for forced current gain A_I of the three circuits shown in Fig. 4-33. Although the value of $V_{CB(sat)}$ affects the magnitude of current

gain in the common-base and modified-common-emitter circuits, this voltage drop is considered sufficiently small to be safely neglected in the following expressions.

Common Base:

$$A_I = \frac{R_E V_{CC}}{(V_1 - V_{BE(ON)})R_L} \tag{4-67}$$

Modified Common Emitter:

$$A_I = \frac{1}{1 + R_L(V_1 - V_{BE(ON)})/R_B(V_{CC} + V_1 - V_{CE(sat)})} \tag{4-68}$$

Common Emitter:

$$A_I = \frac{R_B(V_{CC} - V_{CE(sat)})}{R_L(V_1 - V_{BE(ON)})} \tag{4-69}$$

Equations (4-67) and (4-68) are valid only when α_N is at least as large as the calculated value of A_I. The value of β_N must be at least as large as the A_I value determined from Eq. (4-69) in order for this latter expression to be valid.

Switching Response. Switching response of the common-base stage is superior to that of the modified-common-emitter and common-emitter circuits. Mathematically, these latter two circuits have identical switching speeds, although collector-base capacitance may cause the modified-common-emitter circuit to turn on faster than the common-emitter stage.

4-9. BASIC APPLICATIONS OF TRANSISTOR SWITCHES

Many varieties of transistor switches have been used in switching applications. A large number of saturated switching circuits contain one or more common-emitter, modified-common-emitter, or common-base stages. The purpose of this section is to describe basic applications of these three circuits. Later chapters elaborate upon certain of these applications by providing design examples of single-transistor switching stages and also by combining various stages to form more complex circuits.

A transistor switch can be used to control current flow in an external load. One very important consideration in the application of transistor switching circuits is the manner in which the external load is connected to the transistor. An external load can be connected to the collector terminal of the three circuit types referred to above (and also to many nonsaturating switches) in one of the following modes:

1. The load is in series with the collector terminal and supply voltage. Collector-current flow permits a current flow through the load.
2. The load is in parallel with the collector and emitter terminals; a series resistor is placed between the collector terminal and supply voltage. Current flows into the load only when collector current does not flow. When the transistor is turned on, current is steered from the external load and into the collector terminal.

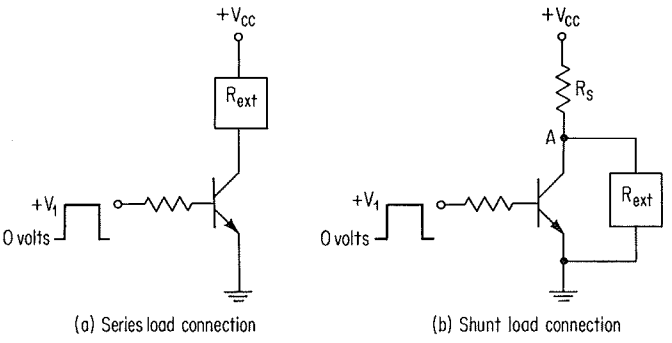

Fig. 4-34. Two types of load connection.

Figure 4-34 shows these two types of load connection for the common-emitter stage; the load is designated R_{ext}. Current through R_{ext} in Fig. 4-34*a* is identical to collector current of the transistor. When the transistor in Fig. 4-34*b* is not conducting, current flows from node A into R_{ext}, as this is the only path for current flow. When the transistor conducts, current at node A flows into the collector of the transistor, as the saturated switch presents a lower impedance to current flow than R_{ext} does. Collector current in this latter circuit is larger than the current flow through R_{ext}.

The preceding analysis shows that current flow into an external load can be controlled by two different methods. The particular type of external-load connection depends upon the circuit application. As an example of the series type of load connection, consider that it is desired to light a lamp whenever an input signal becomes positive. This can be achieved by substituting the lamp for R_{ext} in the circuit given in Fig. 4-34*a*, assuming of course that input-current and transistor-current gain can provide sufficient current to the lamp.

Consider, however, in the foregoing example, that the transistor has a β_N of 20, a base current of 1.0 ma is available, and the lamp requires 100 ma of current. The simple series load connection described above is not sufficient to light the lamp. Two slightly more complex circuits can be used to provide sufficient current to the lamp. Additional transistor stages, cascaded as shown in Fig. 4-35, provide increased current flow through the lamp. Resistor R_{L1} can be chosen

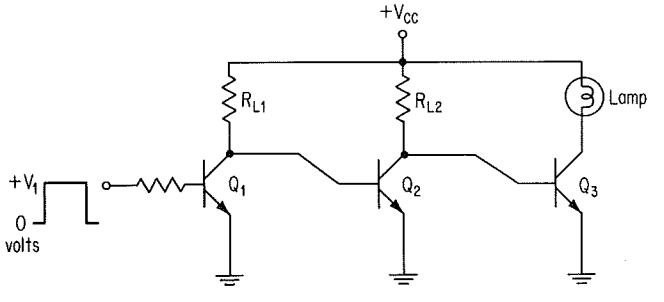

Fig. 4-35. Cascaded stages for increased current gain.

such that collector current of transistor Q_1 is slightly less than the product of input current and β_N of this transistor. Current is steered into the base of transistor Q_2 whenever Q_1 is not conducting. Base current to Q_2 is nearly as large as collector current of Q_1; current gain of Q_2 should enable the collector current of this second inverter to light the lamp. However, an additional stage of inversion is provided by transistor Q_3 in order for the lamp to light when the input signal is positive.

A second circuit approach to increase current flow through the lamp is shown in Fig. 4-36. Collector current of the N-P-N transistor flows principally through the base-emitter diode of the P-N-P device. Except for a small current which flows through the 10-kilohm resistor, base current of the P-N-P transistor can be as large as the circuit input current multiplied by β_N of the N-P-N transistor. Current gain of the P-N-P device enables sufficient current to flow through the lamp.

An example of the shunt connection of the lamp is shown in Fig. 4-37. Current through R_{L2} is steered either into the collector of transistor Q_2 or into the lamp. Because of series resistance R_{L2}, the value of V_{CC} must be larger than it was in the circuits of Figs. 4-35 and 4-36. When Q_2 of the present circuit turns on, considerably more current flows through this device than flowed through the output transistor in either of the two previous circuits.

Although the above examples describe circuits for lighting a lamp, the same principles of operation apply to circuits which drive other types of load. In many instances, the load is one or more transistors. This is particularly true in logic-circuit applications; circuits of this type are described in Chap. 10. Either of the three saturated circuit types described in this chapter can be used to drive an external load. Certain features of each circuit type are described below.

Common-emitter Circuit. A large collector current can be controlled by a relatively small base current in the common-emitter switch. Individual stages can be cascaded, as shown in Fig. 4-35, to provide increasingly larger output currents.

Common-base Circuit. A negative-input signal is required to drive the N-P-N common-base stage. Collector voltage of this circuit cannot become sufficiently negative to drive an identical stage. One manner in which common-base stages

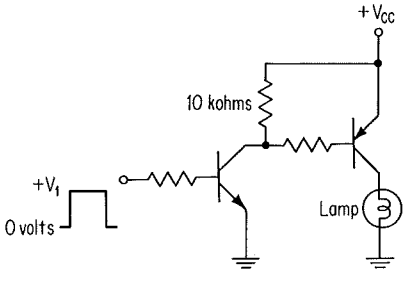

Fig. 4-36. Opposite-polarity transistors connected for large current gain.

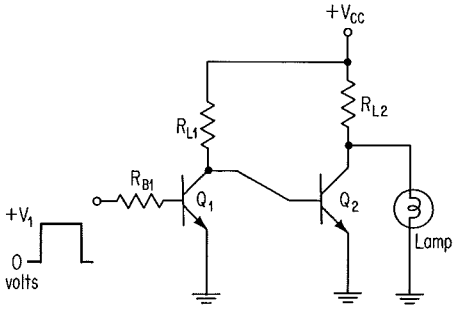

Fig. 4-37. Shunt connection of lamp.

can be cascaded is by use of transformer coupling between stages. This allows the collector voltage swing to be shifted to a more negative level and thus drive the next stage. Current gain of the transformer must be greater than unity to compensate for the less-than-unity current gain of the grounded-base transistor. Although the use of transformer coupling causes a change in state of the transistor during a switching interval, this method of connecting stages cannot keep the transistor in the new state under steady-state conditions.

One application of the common-base switch is as an impedance transformer. Currents of nearly the same magnitude flow in the external circuitry connected to collector and emitter terminals of the device. However, the impedance levels at these two terminals may differ considerably from each other. Thus, this circuit can switch a fixed current from one impedance level to another.

Modified-common-emitter Circuit. Figure 4-7 shows that the output signal of a modified-common-emitter stage is of the correct polarity to drive an identical stage. However, because current gain of this circuit is less than unity, successive stages in a cascaded arrangement would each conduct less current than the previous stage. One application of the modified-common-emitter circuit is to provide both positive and negative output signals at the collector terminal.

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5

The Transistor Data Sheet

5-1. DATA-SHEET INFORMATION

In general, the transistor data sheet provides information on physical and electrical properties of a transistor. The class, or type, of transistor is usually indicated on the data sheet and reveals the fabrication process used to construct the device. A second physical aspect of the transistor is given by an outline drawing showing the size of the header and location of the emitter, base, and collector terminals. Electrical characteristics of a transistor, rather than these physical properties of the device, are of more concern to the circuit designer. The data sheet presents both dc and ac electrical characteristics of a transistor. Certain of these electrical parameters are considered in the remainder of this chapter.

It is not practical for a data sheet to list values for a large number of dc and ac parameters of a transistor. Generally, the parameters listed are those considered most relevant to the class of application for which the transistor was designed. The discussion of data-sheet parameters in this chapter is limited to those electrical characteristics which are important in switching-circuit design.

Strictly speaking, the value of an electrical parameter has no significance unless the test conditions are specified. The discussion of Sec. 2-3 pointed out that small-signal (ac) parameters of a device are dependent upon operating dc current and voltage levels. In a similar manner, large-signal (dc) parameters of a transistor are affected by dc current and voltage levels. When one speaks of any parameter of a transistor without specifying the test conditions, the implication is that the particular measurement is made within a certain limited range of voltage and current levels which have become generally accepted as test conditions for that parameter.

Electrical characteristics may vary widely among transistors of the same type, including those units which were fabricated in the same batch. Because of this, the data sheet lists a typical, minimum, or maximum value, or any combination of the three values, for a given parameter.

Certain transistor parameters are often measured, for a constant temperature, over a range of dc operating levels. Information obtained from these tests is usually presented in the form of plotted curves. These curves are considered to

be typical for the particular device. Also, current and voltage levels can be maintained constant and a parameter measured over a range of operating temperatures. Typical curves can also be shown for these latter measurements.

5-2. VALUE OF DATA SHEET

Information presented on the data sheet is intended as a guide for transistor selection. Breakdown-voltage ratings and leakage-current magnitudes show the range of voltage levels for which the transistor will operate satisfactorily. Transistor voltage drops, dc current gain, and certain of the ac parameters may also be useful in selecting a transistor for a particular application. Current and voltage levels for which data-sheet parameters are given usually do not correspond to the current and voltage levels of the intended application. Often, however, adequate information can be obtained from the plotted curves showing electrical characteristics for various current and voltage levels.

Data-sheet information enables a comparison to be made among various transistor types. Many of the electrical parameters cannot be compared directly, because of differences in voltage and current levels at which like parameters are measured. Where differences in levels of measurement are slight, one transistor can be accurately contrasted to another. In those instances where there are large differences between levels of measurement, the circuit designer can obtain only approximate comparisons.

5-3. PREPARATION OF A DATA SHEET

Consider that a semiconductor manufacturer has developed a transistor and, now that units are being fabricated on a large scale, wishes to provide a data sheet for the device. This data sheet is to characterize the transistor adequately for a particular application. The decision must be made as to which parameters are to be included in the data sheet, together with conditions of measurement for each of the parameters. There is a certain amount of background information which is useful in this consideration. Certainly there must be a potential market for the device; otherwise, it would not have been manufactured. Various groups within the company structure, such as field sales, marketing, and applications engineering, have shown the need for such a transistor and have presented device engineering with a list of desired electrical characteristics for the unit. The choice of parameters to be included in the data sheet is based largely upon these listed electrical characteristics, although the exact levels of current and voltage at which measurements are to be made may not yet be determined for all parameters. Feasibility of the transistor has been shown by device engineering, which has designed the transistor, built several units on a small scale in pilot production, and transferred the fabrication process to a production line. Many measurements have been made on the developmental transistors during the early stages of device design and pilot production. These measurements were necessary to determine how well the actual devices met the desired electrical specifications. The results of these measurements usually determine conditions of measurement for the production devices.

In order for a data sheet to be representative of a production run of transistors, measurements must be made on a large number of devices. Electrical characteristics of at least 100 transistors should be obtained. The results of these measurements show that, for any individual parameter, there is a distribution of values among the various devices. As an example of this distribution, consider that I_{CBO} measurements are made on 100 N-P-N germanium-alloy transistors at a collector-base voltage of +20 volts. The distribution of parameters can be plotted as shown in Fig. 5-1. The horizontal scale is divided into increments of 1μa; the number of transistors having an I_{CBO} magnitude falling within any increment is indicated by a plotted point at the high edge of that increment. Thus, for this example, there are 60 transistors having an I_{CBO} value greater than 3 μa but not greater than 4 μa. A smooth curve joins the plotted points and shows the distribution of parameters.

Distributions can be plotted for each of the measured parameters. These distributions are used to determine values to be listed on the data sheet. For certain parameters, only a maximum value is usually shown on the data sheet. For other parameters, only a minimum value is normally given, and for still other parameters, often only a typical value is listed. In some instances, typical, maximum, and minimum values are shown for a parameter.

For a normal distribution, there is a trailing off of the curve on either side of the peak; the majority of measured values are within a rather limited range of the distribution. A maximum or minimum value for a data-sheet parameter usually does not include the entire distribution. As an example of this, consider the I_{CBO} distribution shown in Fig. 5-1. If the transistor manufacturer specified a maximum I_{CBO} of 10 μa, it would be expected that all future transistors manufactured in the same manner as the 100 evaluation units would meet this specification. However, the distribution shows that 97 per cent of the manufactured devices have an I_{CBO} value not greater than 6 μa. The manufacturer can offer a superior device by rejecting 3 per cent of the completed units.

In some instances, the semiconductor manufacturer cannot arbitararily decide upon the maximum value or minimum value of a data-sheet parameter. If marketing has stated that the transistor of the above example must have a maxi-

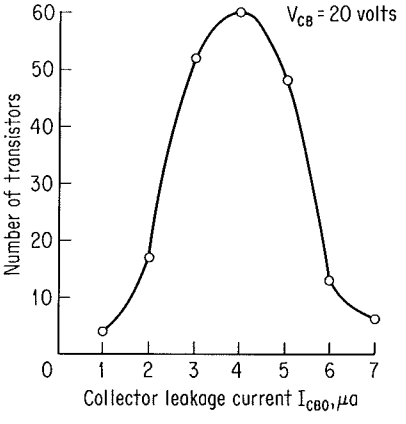


Fig. 5-1. Distribution plot of I_{CBO}.

mum I_{CBO} rating of 4 μa in order to be salable, there is little choice but to specify this 4-μa level. The manufacturer now experiences a yield loss of 34 per cent as determined from the distribution plot of Fig. 5-1.

Once a data sheet has been prepared, the transistor can be registered with the Joint Electron Device Engineering Council (JEDEC). The transistor is assigned an identifying code name consisting of the prefix 2N followed by two or more numbers. For instance, one type of N-P-N germanium-alloy transistor is designated 2N1302.

Guaranteed data-sheet electrical parameters, together with certain mechanical specifications, identify a registered device. Any semiconductor manufacturer may sell transistors having the same registration number, provided that electrical and mechanical characteristics of the devices correspond to data-sheet values of the registered transistor.

The following three sections of this chapter discuss data-sheet parameters. In order to illustrate the various electrical characteristics presented on a typical data sheet, parameter values are shown for an N-P-N germanium medium-power switching transistor. The given data do not apply to any single transistor, although values are similar to those of many actual devices.

5-4. ABSOLUTE MAXIMUM RATINGS

Maximum limits of operation exist for all electronic devices. Maximum operating limits for the transistor are listed on the data sheet under the heading *absolute maximum ratings.* The device manufacturer does not guarantee satisfactory operation of the transistor if these limits are exceeded.

Table 5-1 presents absolute maximum ratings of the representative transistor. The first five ratings are specified at an ambient temperature of 25°C. This temperature level corresponds closely to that of a comfortable level for the human environment and is typically a standard value chosen for many dc and ac electrical specifications of transistors.

Table 5-1. Absolute Maximum Ratings at 25°C Ambient Temperature (Unless Otherwise Noted)

Collector current	150 ma
Collector-base voltage	20 volts
Collector-emitter voltage*	12 volts
Emitter-base voltage	3.0 volts
Total device dissipation at 25°C ambient temperature†	150 mw
Total device dissipation at 25°C case temperature‡	300 mw
Collector-junction temperature	+85°C
Storage-temperature range	−65 to +100°C

* For an open-circuited emitter-base diode.

† Derate linearly to 85°C ambient temperature at the rate of 2.5 mw/°C.

‡ Derate linearly to 85°C case temperature at the rate of 5 mw/°C.

No conditions of measurement are given for either the absolute maximum current or absolute maximum voltage ratings. The absolute maximum collector-current level is considered to be the largest value of dc collector current which the transistor can safely conduct, regardless of other voltage and current levels associated with the device. An increase of current beyond this level can be expected to cause degradation of the unit. The absolute maximum voltage ratings can usually be exceeded, *provided* that the resultant currents cause only a small power dissipation in the device. In many circuit applications, there may be no current-limiting resistor. For this reason, the above voltage ratings are considered to be absolute maximum values. The first footnote to Table 5-1 states that collector-emitter voltage is specified for an open-circuited emitter-base diode; this gives the lowest breakdown-voltage rating ($V_{(BR)CEO}$) between collector and emitter terminals.

Maximum power dissipation is given for two conditions of operation. The first of these ratings is shown as total device dissipation at 25°C ambient temperature. Dissipation rating of the transistor is based upon a maximum allowable collector-base junction operating temperature. The device under consideration can safely dissipate 150 mw when operated in a room-temperature environment. The transistor header transfers a sufficient amount of generated heat to the air, and temperature of the collector-base junction does not become excessive. At free-air temperatures above the 25°C level, a smaller amount of heat is transferred to the air, and the maximum power dissipation is reduced. Figure 5-2 shows two curves of maximum power dissipation versus temperature. The curve labeled ambient temperature shows the allowable device dissipation at free-air temperatures above the 25°C level. Allowable device dissipation is seen to be zero at a free-air temperature of 85°C. The second footnote of Table 5-1 states that maximum power dissipation must be derated linearly to 85°C ambient temperature at the rate of 2.5 mw/°C. This derating constant is simply the negative slope of the dissipation curve.

A second dissipation rating applies to the transistor *only* when temperature of the header is maintained at 25°C. This rating is listed in Table 5-1 as total device dissipation at 25°C case temperature. The transistor of this discussion can

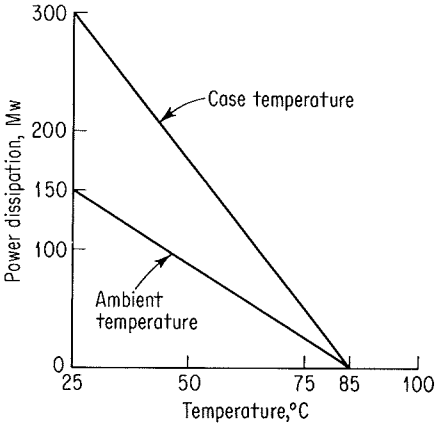


Fig. 5-2. Plots of maximum power dissipation versus temperature.

dissipate 300 mw at the 25°C case temperature. In order to maintain the above temperature level, the transistor case must be attached to an "infinite" heat sink. For many practical applications, the infinite heat sink is simulated by a metal plate having a large surface area. More power can be dissipated at a case temperature of 25°C than for the 25°C free-air operating condition. The derating curve to be used for various case temperatures is shown in Fig. 5-2 as the plot labeled case temperature. This curve has a larger slope than the curve associated with free-air temperatures; the derating constant for various case temperatures is given in the third note as 5 mw/°C. Both derating curves are seen to allow zero dissipation at the 85°C point.

Maximum collector-junction temperature is shown in Table 5-1. Maximum power-dissipation ratings are based upon this allowable junction temperature, although the temperature itself is usually of little concern to the circuit designer. This collector-junction temperature rating is often omitted from data sheets.

Storage-temperature range is an important consideration in the application of transistors. This rating is given in Table 5-1 as -65 to $+100$°C.

Absolute maximum ratings are important as a guide to limits of transistor operation. A consideration of these ratings assists in selecting a device for a particular dc application. However, a much more detailed examination must be made of various dc and ac electrical characteristics before a transistor is selected for a particular application. The following section describes these additional electrical characteristics.

5-5. ELECTRICAL CHARACTERISTICS

Table 5-2 shows several dc and ac electrical characteristics of the transistor. The listed parameters are intended to characterize the device for use in switching-circuit applications. Except where noted, the parameters are given for an ambient temperature of 25°C.

Leakage Currents, Breakdown Voltages. Nomenclature for leakage currents and breakdown voltages was presented in Chap. 1. Curves *A* and *B* of Fig. 5-3

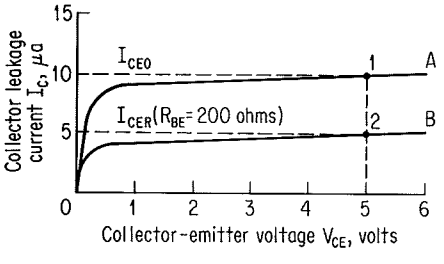


Fig. 5-3. Collector leakage currents for low values of applied voltage.

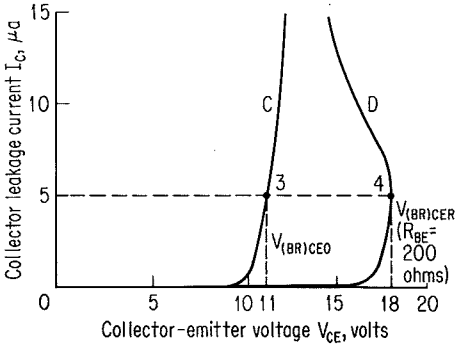


Fig. 5-4. Collector breakdown characteristics.

Table 5-2. Electrical Characteristics at 25° Ambient Temperature (Unless Otherwise Specified)

Parameter		Test conditions			Min.	Typ.	Max.	Unit
I_{CBO}	Collector cutoff current	$V_{CB} = 15$ volts	$I_E = 0$		...	0.3	0.5	μa
I_{CEO}	Collector-emitter leakage current	$V_{CE} = 5$ volts	$I_B = 0$		...	....	10	μa
I_{CER}	Collector-emitter leakage current	$V_{CE} = 5$ volts	$R_{BE} = 200$ ohms	$I_B = 0$	...	....	5	μa
$V_{(BR)CBO}$	Collector-base breakdown voltage	$I_C = 100$ μa	$I_E = 0$		20	....	....	volts
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	$I_C = 5$ μa	$I_B = 0$		11	....	....	volts
$V_{(BR)CER}$	Collector-emitter breakdown voltage	$I_C = 5$ μa	$I_B = 0$	$R_{BE} = 200$ ohms	18	....	....	volts
$V_{(BR)EBO}$	Emitter-base breakdown voltage	$I_E = 100$ μa	$I_C = 0$		3	....	....	volts
h_{FE}	Dc forward-current-transfer ratio	$V_{CE} = 1.0$ volt	$I_C = 10$ ma		40	60	....	....
h_{FE}	Dc forward-current-transfer ratio	$V_{CE} = 1.0$ volt	$I_C = 10$ ma	$T = -55°C$	20	30	....	....
$V_{CE(sat)}$	Collector-emitter saturation voltage	$I_C = 10$ ma	$I_B = 0.5$ ma		...	....	0.2	volts
V_{BE}	Base-emitter voltage	$I_C = 10$ ma	$I_B = 0.5$ ma		...	....	0.4	volts
$\|h_{fe}\|$	Ac common-emitter forward-current-transfer ratio	$I_C = 10$ ma	$V_{CE} = 10$ volts	$f = 100$ Mhz	4	....	....	....
C_{ob}	Common-base output capacitance	$V_{CB} = 5$ volts	$I_E = 0$	$f = 1$ Mhz	...	3	5	pf

are determined from the I_{CEO} and I_{CER} ratings, respectively, of Table 5-2. For an open-base connection of the transistor, a plot of I_C versus V_{CE} must pass below (or through) point 1 of curve A. Similarly, for a resistor of 200 ohms connected across the emitter-base diode, a plot of I_C versus V_{CE} will not pass above point 2 of curve B.

Figure 5-4 shows collector breakdown curves for the transistor. Point 3 of curve C is determined from the $V_{(BR)CEO}$ value listed on the data sheet. For a common-emitter circuit configuration in which the emitter-base diode is reverse-biased, externally short-circuited, or shorted through a resistor, a plot of I_C versus V_{CE} would exhibit breakdown at a larger value of voltage than the $V_{(BR)CEO}$ level. Curves of this latter type often have a negative slope at high current levels and become asymptotic to the open-base breakdown-voltage level. Curve D shows this characteristic for the transistor under discussion; a 200-ohm resistor is connected across the emitter-base junction of the device. The $V_{(BR)CER}$ level (point 4) is determined from the data sheet.

DC Forward Current Gain. Large-signal dc forward current gain of a transistor is indicated on the data sheet as h_{FE}. This parameter is also termed the "*dc forward-current-transfer ratio*" and is identical to β_N described in Sec. 1-6. Although this current gain is listed on data sheets as a large-signal h parameter, the term is often referred to verbally as "beta."

The above current gain is measured at a convenient level of collector current typically from 10 to 50 ma for medium-power transistors. The transistor must be kept out of saturation for the h_{FE} measurement. Otherwise, there could be several values of I_B for the same I_C, and the ratio of I_C to I_B would not necessarily be the true current gain of the transistor. The collector-emitter voltage level for this measurement is typically from 0.5 to 1.0 volt for medium-power switching transistors.

Collector-emitter Saturation Voltage. Saturation-voltage drop of a transistor in the common-emitter configuration is an important consideration in switching-circuit design.* This saturation voltage, $V_{CE(sat)}$, is often measured at the same level of collector current as used for the h_{FE} measurement. However, apparent current gain of the transistor is now smaller than the listed h_{FE} value. The transistor used for the present discussion has a minimum h_{FE} of 40 at 10 ma (at 25°C) but is biased with a base current of 0.5 ma for the $V_{CE(sat)}$ measurement. A forced current gain of 20 is used for this latter measurement. When designing the above transistor into a switching circuit, current gain of the device must be considered as not larger than 20 if the saturation-voltage level of 0.2 volt is desired. If a minimum current gain of 40 is used for design, there is no assurance that the magnitude of collector-emitter voltage will be below the 1.0-volt level at which the current gain of 40 is specified.

Base-emitter Voltage. Forward voltage drop of the base-emitter diode is listed as V_{BE}.† This parameter is usually measured at the same levels of collector and base currents as used for the $V_{CE(sat)}$ measurement.

* Refer to Sec. 1-7 for a discussion of this parameter.

† The term $V_{BE(ON)}$ is generally used throughout the text for V_{BE}.

Small-signal Current Gain, Cutoff Frequency. The absolute value of h_{fe} is shown in Table 5-2.* This parameter, defined in Eq. (2-2) as the ratio of i_c to i_b, is designated "ac common-emitter forward-current-transfer ratio." The parameter is determined by forward-biasing the base of a grounded-emitter stage and measuring magnitudes of base and collector currents. An ac short circuit exists across the collector-emitter terminals for this measurement.

Small-signal collector-current amplitude of the common-emitter stage is expressed in Eq. (4-46) as a function of current gain, base current, input frequency, and a common-base cutoff frequency. This equation is valid for $Z_c \gg Z_L$ and gives a relationship between output current, input current, and input-signal frequency. Both sides of Eq. (4-46) can be divided by i_c to give the ratio i_c/i_b; substitution of the left side of Eq. (2-2) for i_c/i_b yields, after slight manipulation,

$$h_{fe} = \frac{a_o}{(1 - a_o)\left[1 + j\dfrac{f}{(1 - a_0)f_a}\right]} \tag{5-1}$$

where $$f = \frac{\omega}{2\pi} \qquad f_a = \frac{\omega_a}{2\pi}$$

A plot of the above equation, for various values of f, is shown by the solid line in Fig. 5-5. The curve has been adjusted to correspond to the minimum values given in Table 5-2 for h_{FE} and $|h_{fe}|$. Amplitude of h_{fe} is shown along the ordinate axis in decibels; low-frequency amplitude of this parameter is considered equal to h_{FE} of Table 5-2 and is shown as 32 db (numerically equal to 40). Frequency f is plotted along the abscissa to a log scale. At a frequency of 100 Mhz, $|h_{fe}|$ is shown as 12 db (numerically equal to 4) to correspond to the data-sheet value for this parameter. The f_a term of Eq. (5-1) is determined to equal 410 Mhz for the data-sheet transistor. This transistor has an a_o value of 0.9757.

At low frequencies, $f \ll f_a$, and Eq. (5-1) reduces to

$$h_{fe} = \frac{a_o}{1 - a_o} \tag{5-2}$$

Current gain given by the above equation is approximately equal to h_{FE} of the transistor. As input frequency increases, the $f/(1 - a_o)f_a$ term of Eq. (5-1)

* Parameter h_{fe} is described mathematically as a complex quantity. The absolute-value designation indicates that the magnitude of h_{fe} is given.

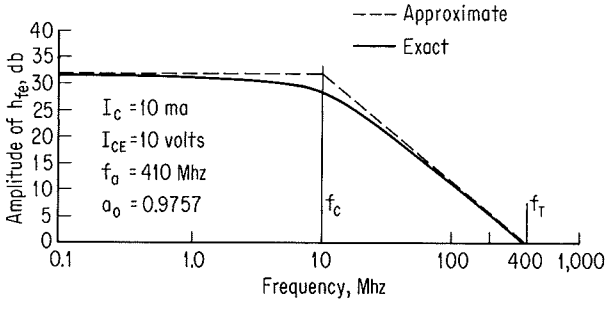


Fig. 5-5. Approximate and exact variation of h_{fe} versus frequency.

becomes dominant, and amplitude of h_{fe} begins to decrease. At input frequencies such that $f \gg (1 - a_o)f_a$, h_{fe} is determined from Eq. (5-1) to be approximately

$$h_{fe} = \frac{a_o}{jf/f_a} \tag{5-3}$$

The dashed line shown in Fig. 5-5 is determined from Eqs. (5-2) and (5-3). The horizontal portion of the line is a plot of Eq. (5-2) to f_c, the frequency at which the real and imaginary terms of Eq. (5-1) are equal. Frequency f_c is given by

$$f_c = f_a(1 - a_o) \tag{5-4}$$

and is referred to as the "break" or "corner" frequency of the dashed-line plot. Equation (5-3) is plotted from f_c to f_T. This latter frequency is defined to be the value of f at which h_{fe} is equal to unity (0 db). The slope of the dashed-line plot beyond f_c is -6 db/octave.

Figure 5-5 shows that, except in the vicinity of f_c, the actual frequency-response plot of h_{fe} lies close to the dashed-line plot. The solid curve is asymptotic to the dashed line at low and high frequencies. At $f = f_c$, h_{fe} is determined from Eqs. (5-1) and (5-4) to be

$$h_{fe} = \frac{a_o}{1 - a_o} \frac{1}{1 + j} \tag{5-5}$$

Amplitude of h_{fe} becomes

$$|h_{fe}| = \frac{a_o}{1 - a_o} \frac{1}{\sqrt{2}} \tag{5-6}$$

The true magnitude of h_{fe} is now 0.707 of the low-frequency gain; expressed in decibels, the curve has fallen by 3 db from the low-frequency value. The solid curve is 3 db below the dashed-line plot at $f = f_c$. Maximum separation exists between the two plots at the f_c frequency. This cutoff point is often termed the "beta cutoff frequency" of the transistor.

Frequency-response characteristics of various transistors are often compared. The frequency at which $|h_{fe}|$ becomes unity is one figure of merit of a transistor; this frequency is designated f_T. Consider that $|h_{fe}|$ is measured at a frequency f_1, where $f_1 \gg f_c$. From Eq. (5-3),

$$|h_{fe}|_{f_1} = \frac{a_o f_a}{f_1} \tag{5-7}$$

where $|h_{fe}|_{f_1}$ is the amplitude of h_{fe} at f_1. The above expression can be solved for $a_o f_a$ to give

$$a_o f_a = f_1 |h_{fe}|_{f_1} \tag{5-8}$$

At the frequency f_T, current-gain amplitude is given by

$$|h_{fe}|_{f_T} = \frac{a_o f_a}{f_T} \tag{5-9}$$

where $|h_{fe}|_{f_T}$ is the amplitude of h_{fe} at f_T. Because $|h_{fe}|_{f_T}$ is unity, Eq. (5-9) can

be rearranged to give

$$f_T = a_0 f_a \tag{5-10}$$

Substitution of the right side of Eq. (5-8) into Eq. (5-10) yields

$$f_T = f_1 |h_{fe}|_{f_1} \tag{5-11}$$

The above expression shows that cutoff frequency of a transistor is determined by multiplying the magnitude of h_{fe} by the frequency at which the measurement is made (provided of course that $f_1 \gg f_c$). In the -6 db/octave region, the product of gain times bandwidth is equal to f_T. Hence, this parameter is often referred to as the "*gain-bandwidth product.*"

A frequency of 100 Mhz is used for the h_{fe} measurement of Table 5-2. This frequency is sufficiently large to assure that current-gain magnitude lies along the -6 db/octave slope of the curve. Equation (5-11) is used to calculate an f_T of 400 Mc for the transistor.

Output Capacitance. Capacitance of the collector-base junction is given for an open-circuited emitter junction and a collector-base voltage of 5 volts. This capacitance, termed "common-base output capacitance," is equal to C_c in parallel with a small header capacitance of approximately 0.5 pf.*

5-6. SWITCHING CHARACTERISTICS

Table 5-3 lists maximum switching times for the transistor in a common-emitter circuit configuration. Circuit test conditions are listed in the table and are chosen to represent a typical circuit application of the device. The $V_{BE(OFF)}$ test condition refers to the OFF-state base-emitter input voltage level. Switching parameters t_d, t_r, t_s, and t_f are described in Sec. 4-5. Figure 4-10 shows input and output waveforms for the common-emitter switch and defines the above switching parameters. As defined in Fig. 4-10, t_r is measured along the falling edge of the output-voltage waveform; the converse of this applies to the t_f measurement. Many data sheets reverse the rise- and fall-time nomenclature of Fig. 4-10. In order to avoid uncer-

* Section 2-2 includes a discussion of C_c.

Table 5-3. Switching Characteristics at 25°C Ambient Temperature

Test conditions

$V_{CC} = 6$ volts $\quad R_L = 600$ ohms
$I_{B1} = 1$ ma $\quad I_{B2} = 0.6$ ma
$V_{BE(OFF)} = 0.5$ volt

	Parameter	*Max., nsec*
t_d	Delay time	20
t_r	Rise time	35
t_s	Storage time	15
t_f	Fall time	60

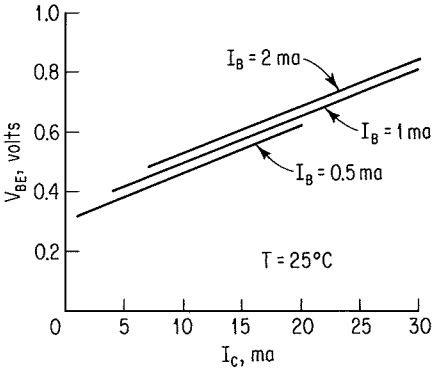


Fig. 5-6. Base-emitter voltage for various base and collector currents.

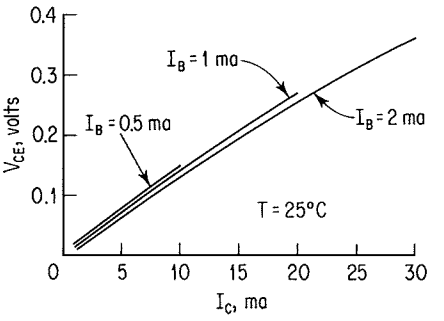


Fig. 5-7. Collector-emitter saturation voltage for various base and collector currents.

tainty in interpretation of the switching measurements, the data sheet normally presents input and output waveforms, together with defined switching parameters. Rise and fall times of the input-voltage waveform are also usually given.

5-7. VARIATION OF DC AND AC PARAMETERS

Most of the parameters listed in Table 5-2 are shown for only one particular operating condition. It may be desirable to know the value of a parameter for various operating conditions. This information is often presented on data sheets by plots of the type shown in Figs. 5-6 to 5-12. These graphical presentations of electrical parameters are considered to be typical for the transistor described by the data sheet.

Figures 5-8 and 5-12 probably require further mention. The first of these figures is a plot of normalized h_{FE} versus temperature. This plotted dc current-gain parameter has been divided by the 25°C typical h_{FE} value listed in Table 5-2. Thus, the plotted value at 25°C has been normalized to unity. In order to obtain

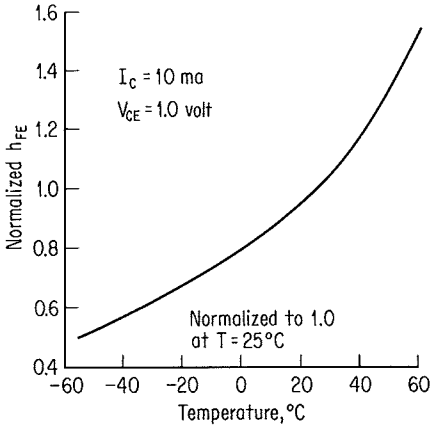


Fig. 5-8. Normalized h_{FE} versus temperature.

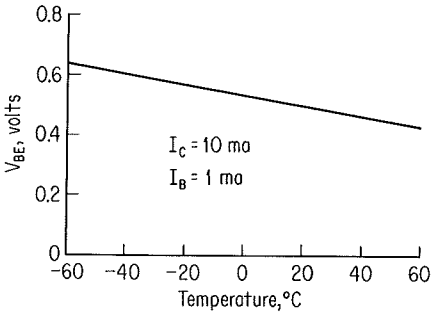


Fig. 5-9. Base-emitter voltage drop versus temperature.

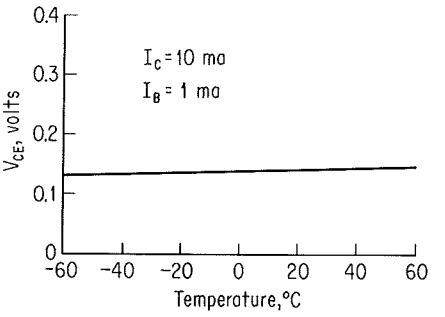


Fig. 5-10. Collector-emitter saturation voltage versus temperature.

the actual value of h_{FE} at any temperature, it is necessary to multiply the normalized value by the typical h_{FE} of 60 listed in Table 5-2.

Contours of constant gain-bandwidth product are presented in Fig. 5-12. These curves show the dependence of f_T upon operating current and voltage levels.

5-8. SPECIAL DEVICES

The transistor-circuit designer may require devices which have slightly superior electrical characteristics to those listed on the data sheet. Because of a distribution of values for any one parameter, it is often possible to screen a production run of transistors to the desired parameter values and thus obtain units having the required electrical characteristics. The transistor manufacturer will often select these premium devices to meet a customer's transistor specifications. These units represent only a small percentage of the production transistors and are more costly than the data-sheet devices.

Many transistors which do not meet data-sheet specifications may be useful in various applications. A particular circuit may not require transistors having all

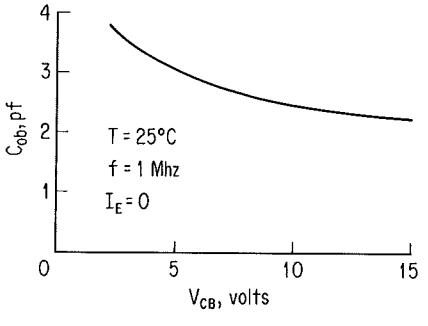


Fig. 5-11. Common-base output capacitance versus collector-base voltage.

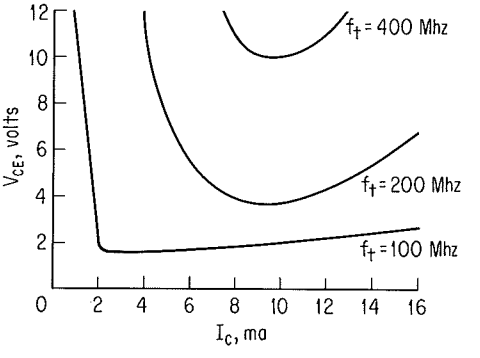


Fig. 5-12. Contours of constant gain-bandwidth product.

the guaranteed electrical characteristics listed on the data sheet. Transistors can be screened by the device manufacturer to relaxed specifications from those shown on the data sheet. This is often done upon request from a customer and can provide usable transistors at a reduction in price from that of the data-sheet units. However, the cost of additional screening may cause the price of these fallout transistors to be near that of the data-sheet units; there may then be no economic justification for use of the fallout devices.

6

Saturated-inverter Design

6-1. INTRODUCTION

Material presented in the preceding chapters has been concerned principally with those physical and electrical characteristics of transistors which are of importance in transistor switching-circuit design. Now that this background material has been presented, it is possible to proceed with a discussion of inverter design, with specific consideration given to base-drive requirements and collector loading. The object of this chapter is to illustrate typical design considerations for four basic types of common-emitter switching circuits which operate from collector-current cutoff to collector-current saturation.

Before proceeding further, it should be noted that exact design rules cannot be presented. In some cases, the designer is free to select the transistor type, magnitudes of supply voltages, and current levels at the base and collector terminals. In other instances, one or more of the above circuit parameters may be fixed, and the resulting design must be within the framework of the given parameters. Because of frequency-response and current-gain limitations of the transistor, in addition to inductive and capacitive effects of circuit wiring, it is not always possible to meet all design objectives. In order to design the best possible circuit, the designer should be aware of the manner in which various device and circuit parameters affect circuit performance. A knowledge of features and limitations of a proposed design will allow various changes to be made in the design before the circuit is actually fabricated.

6-2. BASE-DRIVE CURRENTS, REVERSE-BIAS VOLTAGE

Effects of forward and reverse base-drive currents, as they relate to switching speeds of transistors, have been discussed in Sec. 4-6. It was shown that, in general, turn-on and turnoff times are decreased for an increase in the forward and reverse drive currents, respectively. It is possible to increase either, or both, of these currents so much that the usefulness of the transistor as an amplifying element is reduced, i.e., the control currents approach the magnitude of the current being controlled, and there is little point in placing a transistor in the circuit. In

those designs where switching speed is not important, forward base current need only be large enough to saturate the transistor, and reverse base current can be practically negligible.

For those circuits where low switching times are important, forward and reverse base currents should be larger than that associated with slow-speed switching. As forward base current is increased, the larger overdrive factor causes a reduction in turn-on time. This increased base current gives a smaller value of forced gain for the transistor. Faster turn-on time is thus achieved by designing the circuit to have a smaller value of forced gain. A general rule of thumb is to operate the transistor at a forward gain of from 0.4 to 0.7 times h_{FE} (where h_{FE} is measured at the particular level of collector current). In addition to turning the transistor on more quickly, the relatively large forward base current permits a reasonably low $V_{CE(\text{sat})}$ level.

Figure 6-1 shows an N-P-N inverter circuit in which forward base current I_{B1} is supplied by the input signal and which relies upon a current flow out of the base and through R_B for a reverse base current I_{B2}. For the input-voltage waveform of input A, forward base current is given by Eq. (4-5), or

$$I_{B1} = \frac{V_1 - V_{BE(\text{ON})}}{R_B} \tag{6-1}$$

When the input voltage drops to ground potential, transient current flow out of the base, given by Eq. (4-54), is

$$I_{B2} = \frac{V_{BE(\text{ON})}}{R_B} \tag{6-2}$$

If the voltage waveform of input B is applied to the circuit, forward base current is given by Eq. (6-1), but the expression for reverse base current becomes that of Eq. (4-55), or

$$I_{B2} = \frac{V_2 + V_{BE(\text{ON})}}{R_B} \tag{6-3}$$

For either of the two input waveforms, forward and reverse base currents can be simultaneously increased by a reduction in the value of R_B. An increase of voltage level for V_1, for either input waveform, causes a larger value of I_{B1} without affecting the magnitude of I_{B2}. Similarly, a more negative level for V_2 of input B increases I_{B2} but has no effect upon the magnitude of I_{B1}.

Application of the $-V_2$ voltage level of input B to the above circuit causes a

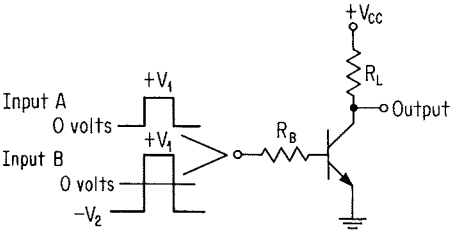


Fig. 6-1. Grounded-emitter switch with typical driving signals.

reverse-bias voltage to exist across the base-emitter junction of the transistor. This off-state base-emitter voltage helps assure transistor cutoff at elevated temperatures. In practice, the level of V_2 should be less negative than the reverse breakdown voltage of the base-emitter diode. If this breakdown voltage is exceeded, a significant amount of reverse current may flow out of the base under steady-state conditions. This current flow, together with the breakdown-voltage level existing across the base-emitter junction, may cause excessive power dissipation in the base-emitter diode.

A second common-emitter inverter is shown in Fig. 6-2. Although the emitter is at a potential of $-V$ volts, ac impedance of the $-V$ voltage supply is ideally zero ohms, and the emitter is grounded for ac, or pulse, input signals. When the input is at ground potential, forward base current becomes

$$I_{B1} = \frac{V - V_{BE(ON)}}{R_B} \tag{6-4}$$

Reverse base current flows when the input drops to $-V_1$ volts and is determined to be

$$I_{B2} = \frac{V_1 + V_{BE(ON)} - V}{R_B} \tag{6-5}$$

provided that $|V_1| \geq |V|$. Voltage $-V_1$ must be at least as negative as the emitter potential $-V$ in order for the transistor to turn off. Variation of either the most positive or most negative input-voltage level to the circuit affects either the forward base current or reverse base current, respectively, but not both. A change in the value of R_B affects forward and reverse base current in the same manner, whereas a change in the level of $-V$ increases one base current and decreases the other.

Reverse-bias voltage of the above circuit is determined principally by magnitudes of $-V_1$ and $-V$. If reverse breakdown voltage of the base-emitter diode is not exceeded, the reverse-bias voltage is given by

$$V_{BE(OFF)} = V - V_1 - I_{BX}R_B \tag{6-6}$$

where $V_{BE(OFF)}$ = OFF-state voltage of the base-emitter diode
I_{BX} = reverse-bias base leakage current

If the above expression yields a more negative voltage level than the actual base-emitter breakdown voltage, the reverse-bias voltage will be clamped to the breakdown-voltage level, and direct current will flow out of the base.

Voltage levels of the emitter and base terminals in the circuit of Fig. 6-2 can be shifted by an amount $+V$ so that the emitter is at ground potential and the input signal varies from $|V| - |V_1|$ volts to $+V$ volts; this is shown in Fig. 6-3. Equations (6-4) to (6-6) are valid for this latter circuit.

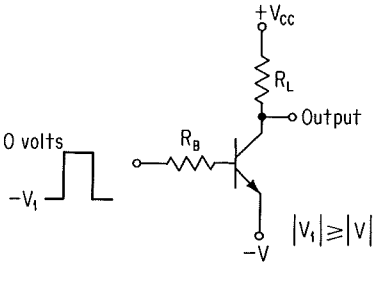


Fig. 6-2. Common-emitter switch with emitter bias.

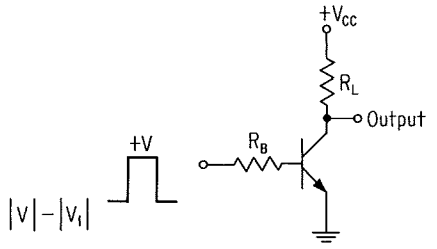


Fig. 6-3. Circuit of Fig. 6-2 with base and emitter potentials shifted by $+V$ volts.

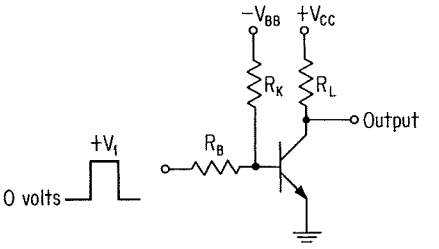


Fig. 6-4. Common-emitter switch with external voltage supply for reverse base drive.

Another common-emitter switching circuit is shown in Fig. 6-4. Forward base current is supplied by the input signal, and reverse base current is supplied primarily by the $-V_{BB}$ supply voltage. Figure 6-5 shows the input portion of the above circuit and is used to determine expressions for I_{B1} and I_{B2}. Figure 6-5*a* shows that current I_1, supplied by the input-voltage source, divides at node A to become I_2 and I_{B1}. It is seen that I_{B1} can be expressed

$$I_{B1} = I_1 - I_2 \tag{6-7}$$

Currents I_1 and I_2 are readily determined in terms of voltages appearing across the two resistors, and forward base current can be described by

$$I_{B1} = \frac{V_1 - V_{BE(ON)}}{R_B} - \frac{V_{BB} + V_{BE(ON)}}{R_K} \tag{6-8}$$

Reverse base current is shown in Fig. 6-5*b* and can be written

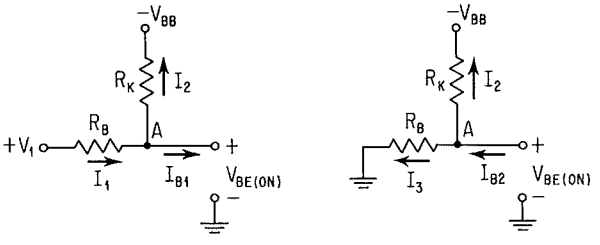
$$I_{B2} = I_2 + I_3 \tag{6-9}$$

Substitution of expressions for I_2 and I_3 into Eq. (6-9) yields

$$I_{B2} = \frac{V_{BB} + V_{BE(ON)}}{R_K} + \frac{V_{BE(ON)}}{R_B} \tag{6-10}$$

Usually the magnitude of I_3 is much smaller than that of I_2, and reverse base current is determined principally by current I_2.

In addition to providing an adequate reverse base drive, the $-V_{BB}$ voltage maintains $V_{BE(OFF)}$ at a negative level and supplies reverse-bias base leakage cur-



(a) Turn-on condition (b) Turn-off condition

Fig. 6-5. Input portion of circuit in Fig. 6-4 for turn-on and turnoff conditions.

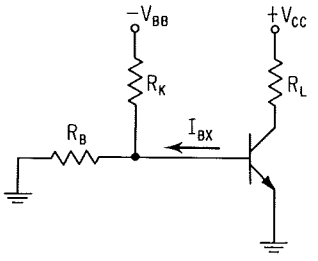


Fig. 6-6. Circuit for determining $V_{BE(OFF)}$ of inverter in Fig. 6-4.

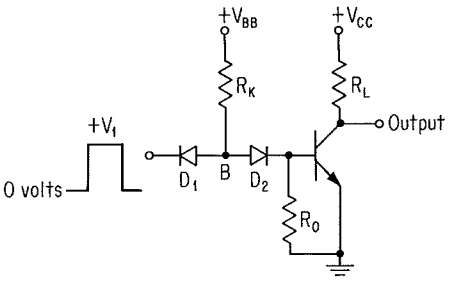


Fig. 6-7. Diode-coupled common-emitter switch.

rent. Reverse-bias voltage is determined from the circuit configuration of Fig. 6-6; this voltage is described by

$$V_{BE(OFF)} = \frac{-(V_{BB} - I_{BX}R_K)R_B}{R_B + R_K} \tag{6-11}$$

Figure 6-7 shows the fourth saturated inverter circuit described in this chapter. Current from the $+V_{BB}$ supply is steered through diode D_1 or diode D_2. When the input signal level is at zero volts, current flows through D_1, and point B is clamped to one diode voltage drop above ground potential. Voltage at point B is now too low to permit current flow through the series combination of D_2 and the base-emitter diode of the transistor; the transistor receives no base drive and is at cutoff. Resistor R_0 serves as a path for collector reverse-leakage current and also provides a path for reverse base current I_{B2}. When the circuit input voltage rises to the base-emitter turn-on voltage, current from point B flows partly through D_1 and partly through D_2, R_0, and the base-emitter diode. As this input-voltage level becomes still more positive, additional current is steered to the right at point B. Diode D_2 eventually conducts all the current away from point B, and the transistor is turned fully on. Forward base current can be expressed

$$I_{B1} = \frac{V_{BB} - V_D - V_{BE(ON)}}{R_K} - \frac{V_{BE(ON)}}{R_0} \tag{6-12}$$

where V_D is the voltage drop of diode D_2. Reverse base current of the circuit is determined to be

$$I_{B2} = \frac{V_{BE(ON)}}{R_0} \tag{6-13}$$

6-3. CONNECTION OF INVERTER STAGES

Equations for base current and reverse-bias voltage presented in the preceding section are useful for transistor stages having precisely defined input-voltage levels. Input signals of this type can be provided by a pulse generator having known terminal voltages. Inverters are often connected so that the output signal of one stage serves as the input signal to a second stage. Input current and voltage levels for this cascade arrangement of inverters are changed from that of a single stage.

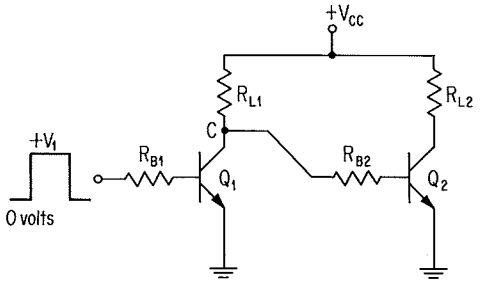


Fig. 6-8. Cascade connection of circuit in Fig. 6-1.

Figure 6-8 shows the cascade connection for two inverters of the type in Fig. 6-1. When transistor Q_1 is at cutoff, current from the V_{CC} voltage source flows through resistors R_{L1} and R_{B2} into the base of transistor Q_2. For Q_1 at cutoff, the input circuit to Q_2 is shown in Fig. 6-9*a*. Current I_{CES} is a reverse collector current of Q_1. Figure 6-9*b* shows the Thévenin equivalent input circuit to Q_2. Forward base current is described by

$$I_{B1} = \frac{V_{CC} - I_{CER}R_{L1} - V_{BE(ON)}}{R_{L1} + R_{B2}} \tag{6-14}$$

Leakage current I_{CER} is usually negligibly small; if this current is neglected, Eq. (6-14) reduces to

$$I_{B1} = \frac{V_{CC} - V_{BE(ON)}}{R_{L1} + R_{B2}} \tag{6-15}$$

A comparison of the above expression with Eq. (6-1) shows the following changes:

1. Input signal V_1 has been replaced by V_{CC}.
2. R_{L1} is now included in the denominator.

Transistor Q_2 in Fig. 6-8 turns off when the signal level at point C drops below the base turn-on voltage level of the device. This occurs when Q_1 saturates, *provided* that the $V_{CE(sat)}$ voltage of Q_1 is below the $V_{BE(ON)}$ threshold level of Q_2. For collector currents below approximately 20 ma, the $V_{CE(sat)}$ voltage of a medium-power switching transistor is usually below the base turn-on voltage level of a similar device. However, as collector current increases, a $V_{CE(sat)}$ level may be reached which will partially or fully turn on a succeeding stage. For $V_{CE(sat)}$

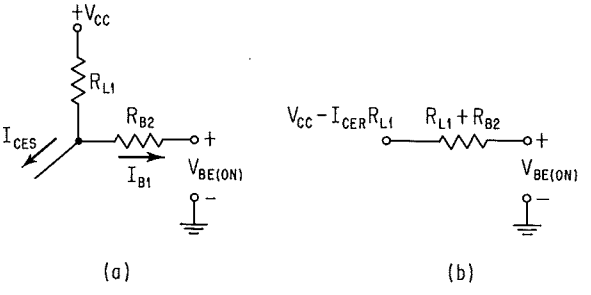


Fig. 6-9. Input circuit to Q_2 in Fig. 6-8 for Q_1 at cutoff.

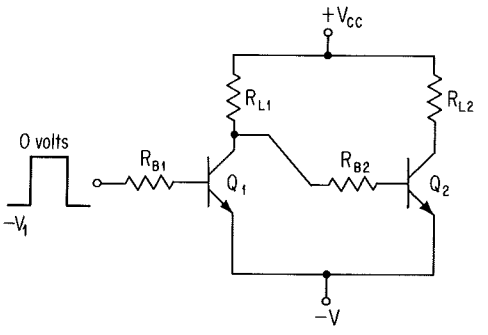


Fig. 6-10. Cascade connection of circuit in Fig. 6-2.

of Q_1 less than $V_{BE(ON)}$ of Q_2 in Fig. 6-8, reverse base current can be expressed

$$I_{B2} = \frac{V_{BE(ON)} - V_{CE(sat)}}{R_{B2}} \tag{6-16}$$

The OFF-state voltage of Q_2 is simply $V_{CE(sat)}$ of Q_1.

Figures 6-10 and 6-11 show the cascade connection for inverters of the type given in Figs. 6-2 and 6-4, respectively. For transistor Q_2 in the circuit of Fig. 6-10,*

$$I_{B1} = \frac{V_{CC} + V - V_{BE(ON)}}{R_{L1} + R_{B2}} \tag{6-17}$$

I_{B2} is given by Eq. (6-16) and

$$V_{BE(OFF)} = V_{CE(sat)} \tag{6-18}$$

Equations for I_{B1}, I_{B2}, and $V_{BE(OFF)}$ for transistor Q_2 in Fig. 6-11 are as follows:

$$I_{B1} = \frac{V_{CC} - V_{BE(ON)}}{R_{L1} + R_{B2}} - \frac{V_{BB} + V_{BE(ON)}}{R_{K2}} \tag{6-19}$$

$$I_{B2} = \frac{V_{BB} + V_{BE(ON)}}{R_{K2}} + \frac{V_{BE(ON)} - V_{CE(sat)}}{R_{B2}} \tag{6-20}$$

$$V_{BE(OFF)} = V_{CE(sat)} - R_{B2}\frac{V_{CE(sat)} + V_{BB}}{R_{B2} + R_{K2}} \tag{6-21}$$

* Collector leakage current is neglected throughout the remainder of this section.

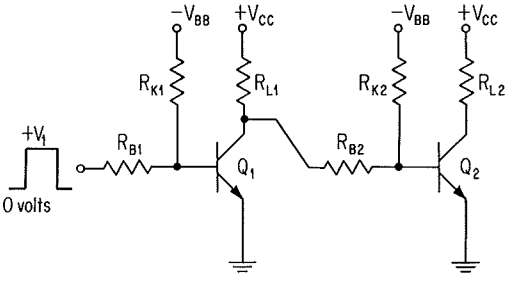


Fig. 6-11. Cascade connection of circuit in Fig. 6-4.

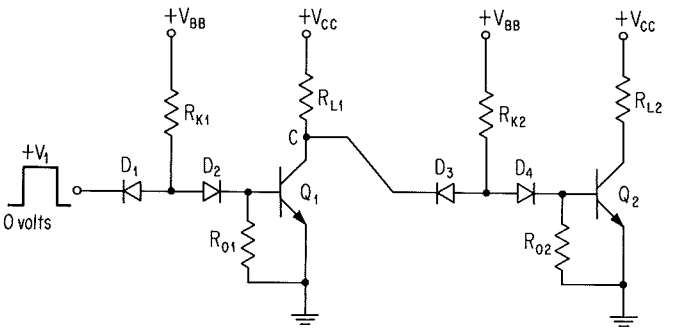


Fig. 6-12. Cascade connection of circuit in Fig. 6-7.

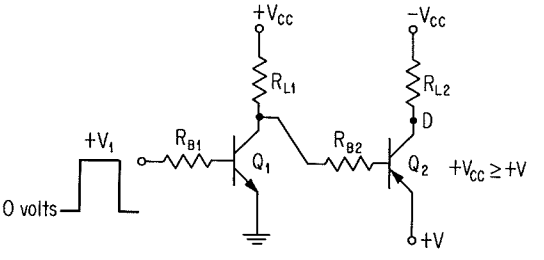


Fig. 6-13. Cascade connection of alternate-polarity transistors.

Inverters of the type given in Fig. 6-7 can be cascaded as shown in Fig. 6-12. Resistor R_{L1} is sometimes omitted in circuits of this type. The presence of R_{L1} allows point C to rise to a positive-voltage level when transistor Q_1 turns off. This resistor is often referred to as a "pull-up" resistor as it "pulls" the collector voltage to a positive level. If R_{L1} is included in the circuit, voltage V_{CC} is usually at least as positive as the V_{BB} supply in order that forward current does not flow through diode D_3 when Q_1 is at cutoff. For $V_{CC} \geq V_{BB}$, forward base current to transistor Q_2 is given by Eq. (6-12). Reverse base current to Q_2 is given by Eq. (6-13). Base voltage of Q_2 in the OFF state is approximately equal to $V_{CE(\text{sat})}$ of Q_1.

Alternate polarity transistors can be cascaded as shown in Fig. 6-13. Transistors Q_1 and Q_2 always have identical conduction modes, i.e., saturation or cutoff. An input signal varying between 0 and $+V_1$ volts is inverted and shifted by the circuit to levels of $-V_{CC}$ and $V - V_{CE(\text{sat})}$ volts at output point D.

6-4. NOISE MARGIN

Noise immunity of an inverter stage is an important consideration in switching-circuit design. Two conditions of noise immunity exist, one for the transistor at cutoff, and one for the device in saturation. Noise immunity is often referred to as noise margin of the circuit. Definitions for the two types of noise margin are given below:

1. *OFF-state noise margin* is the algebraic difference between the minimum voltage level required to turn on the device partially and an applied volt-

age level which does not turn on the transistor. This noise margin is symbolically referred to here as NM_{OFF}.

2. *ON-state noise margin* is the algebraic difference between an applied voltage level which does turn on the transistor and the maximum voltage level required to turn on the device fully. The symbolic representation of this noise margin is NM_{ON}.

As an example of the concept of noise margin, consider the single transistor stage of Fig. 6-1 with input A applied. Let the term $\underline{V}_{BE(ON)}$ represent the minimum value of base-emitter voltage required for any degree of collector conduction greater than the collector cutoff current. Similarly, let the term $\bar{V}_{BE(ON)}$ represent the maximum value of base-emitter voltage required to saturate the transistor. A zero-level input signal to the circuit does not turn on the transistor and, from definition 1 given above, the OFF-state noise margin is written

$$NM_{OFF} = \underline{V}_{BE(ON)} \tag{6-22}$$

The transistor is fully turned on when V_1 is applied; definition 2 above gives the ON-state noise margin as

$$NM_{ON} = V_1 - \bar{V}_{BE(ON)} \tag{6-23}$$

If input B of Fig. 6-1 is applied to the circuit, the OFF-state noise margin becomes

$$NM_{OFF} = \underline{V}_{BE(ON)} + V_2 \tag{6-24}$$

and the ON-state noise margin remains at the level given by Eq. (6-23).

Noise margins associated with coupled circuits are interpreted in the same manner as for a single stage. Consider the cascade circuit of Fig. 6-8. When Q_1 is in saturation, the OFF-state noise margin of Q_2 is given by

$$NM_{OFF} = \underline{V}_{BE(ON)} - V_{CE(sat)} \tag{6-25}$$

The ON-state noise margin of Q_2 is described by

$$NM_{ON} = V_{CC} - I_{CER}R_{L1} - \bar{V}_{BE(ON)} \tag{6-26}$$

Spurious voltage signals caused by induction or by resistive drops in a ground path often appear at the input of an inverter. These noise signals may increase the amplitude of a normally low input signal or may decrease the amplitude of a normally high input signal. The circuit is able to reject noise signals of this nature *only* if noise margin in both the OFF and ON states is larger than amplitude of the noise signals.

6-5. FAN-IN, FAN-OUT

A single inverter stage may control current flow to more than one succeeding stage. In Fig. 6-14, the signal at the collector of transistor Q_1 is fanned out to drive the bases of transistors Q_2, Q_3, and Q_4. The number of stages connected to the output of a single stage is considered to be the fan-out of that particular stage. Thus, Q_1 has a fan-out of 3 in Fig. 6-14. Fan-out is often designated by the symbol N.

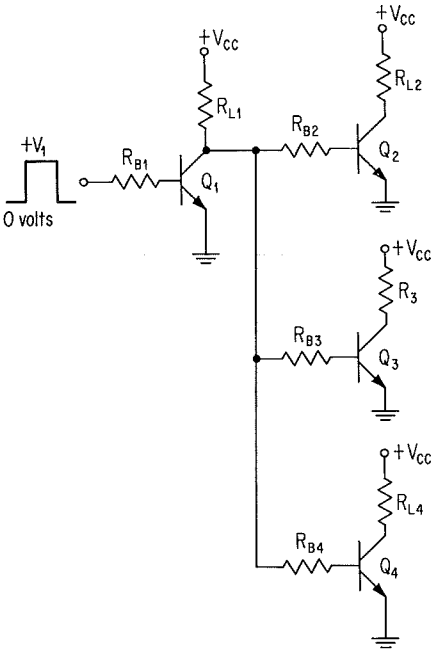


Fig. 6-14. Fan-out of 3 loading at collector of Q_1.

More than one circuit may fan in to the base of a single stage, as shown in Fig. 6-15. When either transistor Q_1, Q_2, or Q_3 is at cutoff, current flows into the base of transistor Q_4. This latter transistor is considered to have a fan-in of 3. The symbol M is often used to represent fan-in.

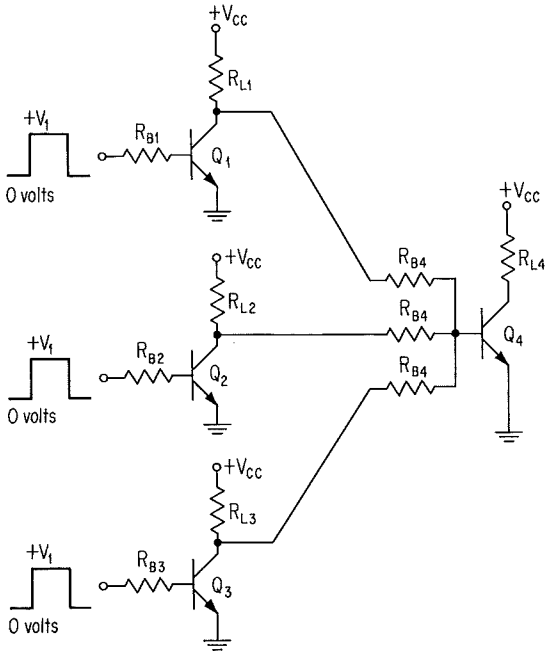


Fig. 6-15. Fan-in of 3 to base of Q_4.

Typical designs are presented in Sec. 6-12 for circuits having a fan-in of unity and a fan-out of either zero or unity. Detailed design considerations involving fan-in and fan-out greater than unity are described in Chap. 10.

6-6. INVERTER AS A CURRENT SINK

The cascaded inverters described in Sec. 6-3 can be grouped into two classes. The first class (class 1) consists of the circuits given in Figs. 6-8, 6-10, and 6-11. In each of these circuits, current through R_{L1} turns on a succeeding stage when Q_1 is not conducting. The circuit of Fig. 6-12 is included in the second class (class 2) of cascaded circuit. This latter circuit does not depend upon current through R_{L1} to turn on a succeeding stage. Rather, resistor R_{K2} supplies required base drive to the second stage.

In circuits of the class 1 type, the transistor collector must conduct current which flows in its own load resistor. This collector current is always larger than the base current which V_{CC} and the load resistor supply to succeeding stages. If additional base current is to be supplied, the required change in V_{CC} or load resistor will cause collector-current flow through the load resistor to increase. A transistor in circuits of the class 2 type is required to conduct current flowing through its own load resistor, in addition to current from all fan-out loads. This current load increases as the fan-out is made larger. Both classes of circuit require the transistor to serve as a current sink. Fan-out from an inverter is limited by the amount of current which the collector can sink and still maintain a sufficiently low value of $V_{CE(sat)}$.

6-7. BASE SPEEDUP CAPACITOR

Voltage and current overdrive to an inverter base can be accomplished with a capacitor connected as shown in the circuit diagram of Fig. 6-16. This capacitor "speeds up" switching transitions of the circuit and is referred to as a "speedup capacitor."

In order to describe circuit effects of the capacitor, it is first necessary to discuss the relation between base voltage and collector-current flow. Generally, base current is considered the controlling input signal to a grounded-emitter stage, with the resulting base voltage dependent upon the amount of emitter current. Actually, emitter current is dependent upon voltage across the base-emitter diode, as described in Sec. 2-2. This current is the result of carrier injection by the emitter and base regions into each other. The majority of those carriers injected into the base travel to the collector region and become collector current. Base current is caused by recombination of emitter-injected carriers in the base region and also by the relatively small amount of carrier injection from base to emitter regions. Col-

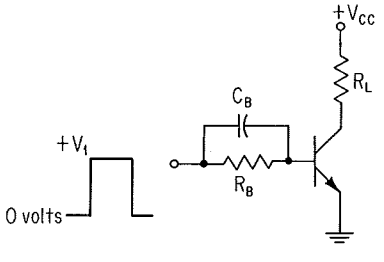


Fig. 6-16. Inverter circuit with base speedup capacitor.

lector current is a result of emitter current and is less than emitter current by the magnitude of base current. Voltage across the base-emitter diode causes emitter-current flow and, consequently, collector-current flow. Base current is a secondary effect of emitter current and represents a departure of the transistor from an ideal voltage-controlled device.

Previous discussions concerning the relationship between base and collector currents are still valid whether one wishes to regard base current or base voltage as the controlling parameter. Consider the grounded-emitter circuit shown in Fig. 6-1. As input voltage is increased above the base-emitter conduction level, base current increases. Base current can also be increased by maintaining input voltage constant (at a positive level greater than that required to turn on the transistor) and decreasing the value of R_B. Both these methods of increasing base current are effective because they increase voltage drop across the base-emitter diode. When the transistor is in saturation, base overdrive is accomplished by causing a relatively large magnitude of base-emitter voltage drop. This voltage increases injected charge from emitter to base regions and provides the base-region carriers for increased collector-current flow. Of course, collector current cannot increase significantly because the transistor is in saturation. Base current increases largely as a result of additional charge in the base region; the overdrive factor [see Eq. (4-32)] increases, and the transistor is considered to be driven harder with base current.

Figure 6-17 shows a circuit representation for the input portion of a common-emitter stage. Impedances Z_i and Z_b represent base-input impedance of the transistor and external series impedance at the base terminal, respectively. Voltage across Z_i is determined by the input-voltage level and by relative magnitudes of Z_i and Z_b. Impedance Z_b can be the parallel resistor-capacitor combination shown in Fig. 6-16. This resistor-capacitor network, together with the small-signal equivalent-circuit representation of Z_i, is shown in Fig. 6-18. Consider that the input-signal level to the latter circuit is initially at zero volts. For a step increase of input voltage, r_b' and the capacitors determine initial voltage distribution in the circuit. If the effect of r_b' is neglected, initial voltage across the base-emitter diode can be expressed

$$v_o = \frac{V_1 C_B}{C_B + C_{se} + C_{te}} \tag{6-27}$$

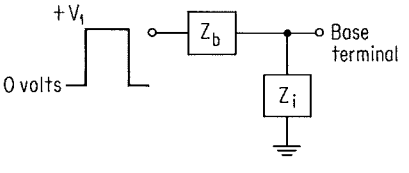


Fig. 6-17. Input circuit of common-emitter stage.

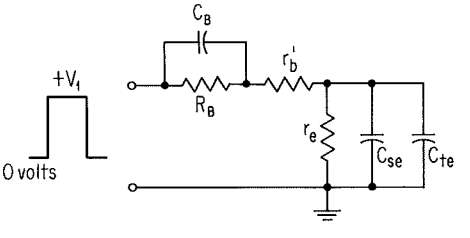


Fig. 6-18. Equivalent input-circuit representation for common-emitter inverter driven by resistor and speedup capacitor.

where V_1 is a step of input voltage. As C_B is made larger, the value of v_o increases to give a larger value of emitter current. Another way of regarding circuit operation is in terms of charge flow into the base. Charging current of C_B flows into the base terminal and charges C_{se} and C_{te}. Larger values of C_B allow more charge to flow and thus turn on the transistor more quickly.

After the input-signal level has been at V_1 volts for a short time, C_B charges, and forward base current is determined by V_1, R_B, r'_b, and the magnitude of $V_{BE(ON)}$. Voltage across C_B is equal to $V_1 - V_{BE(ON)}$ and has the polarity shown in Fig. 6-19*a*. A step decrease of input voltage to zero volts causes the above voltage level across the capacitor to be applied across the base-emitter diode as shown in Fig. 6-19*b*. This relatively large value of reverse voltage causes a large reverse current to flow out of the transistor base, and the device is driven hard to the cutoff state. With respect to charge flow in the circuit, charge across C_B can be considered to cancel out charges across C_{se} and C_{te}.

Realistic input-signal levels do not actually rise or fall in the zero time interval of the assumed step variations in the above discussion. However, input signals to most switching circuits change levels sufficiently fast for the above analysis to apply. The speedup effect of the capacitor is diminished and eventually eliminated as changes of input signal depart more and more from the ideal step variations.

Figure 6-20 shows an input voltage waveform to an N-P-N alloy-junction transistor, together with the resulting base-voltage waveform and output-voltage waveform for various values of base speedup capacitance C_B. The plots show that as C_B is made larger, the base is driven harder for turn-on, and excess base charge is removed more quickly during turnoff. Total switching time of the collector waveform is reduced as C_B is made larger.

In Fig. 6-20, the base-voltage waveform for $C_B = 68$ pf shows that not all excess base charge is removed by the capacitor. The trailing edge of the waveform is the result of a relatively slow decay of excess charge in the base region. The corresponding collector-voltage waveform shows that the transistor partially turns off quickly and then continues to turn off at a slower rate. Excess base charge is completely removed by the 150-pf capacitor. However, discharge time of the capacitor causes a trailing edge of the base-voltage waveform. If the positive-input signal is applied before the capacitor has discharged to zero volts, a portion of the input voltage is canceled by voltage across the capacitor, and a smaller spike of voltage appears at the transistor base; the transistor will now turn on more slowly. Discharge time of a capacitor can be reduced by decreasing the

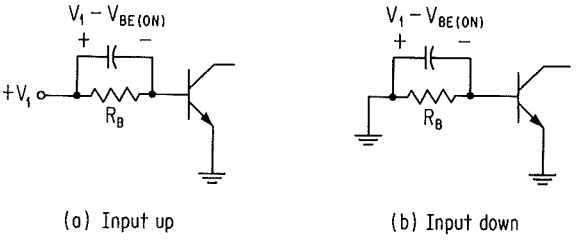


Fig. 6-19. *(a)* **Voltage levels across speedup capacitor for input positive;** *(b)* **input at ground potential.**

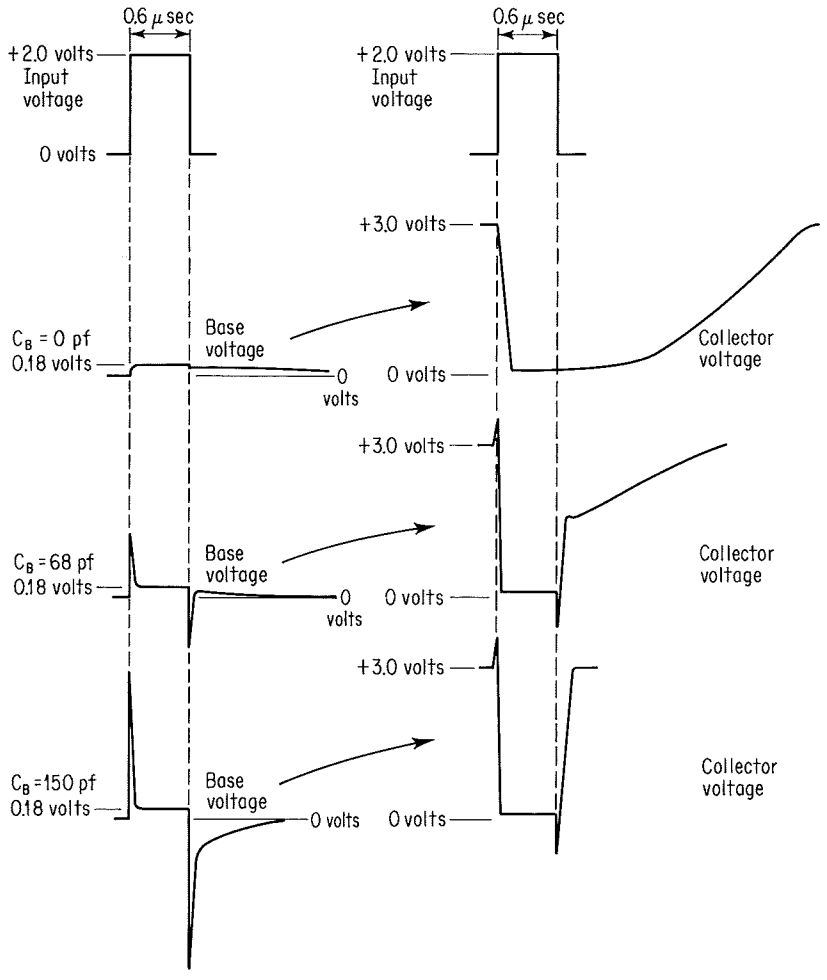


Fig. 6-20. Base and collector voltage waveforms for various values of speedup capacitance.

value of parallel resistor across the capacitor. However, this will allow more dc base current to flow into the transistor; a larger capacitance may then be necessary to remove the increased base charge.

Too low a value of speedup capacitance will not remove sufficient base charge (or collector-stored charge of mesa and planar devices), and turn-on time of the transistor is not significantly reduced. On the other hand, too large a value of speedup capacitor may require a long discharge time, which will increase circuit turn-on time and perhaps restrict repetition rate of the circuit.

The required value of base speedup capacitance is determined by the base-input resistor, collector loading, and type of device. Generally, a larger value of capacitance is used with alloy-junction transistors than with diffused-base mesa or planar devices. Epitaxial diffused-base mesa or planar transistors require the lowest

Table 6-1. Speedup-capacitance Values for Various Types of Switching Transistors

Transistor type	*Typical range of speedup capacitance, pf*
Alloy-junction	35–150
Mesa or planar:	
Nonepitaxial	15–80
Epitaxial	5–20

capacitance values of any device type. Table 6-1 lists typical ranges of speedup capacitance generally used with the above transistor types.

One undesirable feature of a speedup capacitor is its effect upon fall time of a previous stage. The capacitor must charge through R_L of the previous stage and thus increases the fall time of that stage.

6-8. PULSE REPETITION RATES FOR VARIOUS TRANSISTOR TYPES

Total switching time of a circuit is the sum of t_{ON} and t_{OFF} (the sum of t_d, t_r, t_s, and t_f for a saturating circuit). For those circuits where discharge time of a speedup capacitor is not a consideration, it is permissible to apply a turn-on voltage to the circuit immediately after the circuit has turned off. The maximum pulse repetition rate of such a circuit is the reciprocal of the total switching time. This switching time is determined by input- and output-signal levels, the circuit configuration, and characteristics of the transistor itself. It is not possible to give an absolute maximum repetition rate for a device, as a circuit could probably be constructed to give an even higher repetition rate. However, at given levels of saturated collector current, collector load resistance, collector voltage swing, forward base current, and reverse base current, there exist typical values for maximum repetition rate of a transistor.

Figure 6-21 shows typical ranges of pulse repetition rate for various transistors connected in a common-emitter configuration. Saturated collector current is 10 ma, and the collector load resistor is 330 ohms. A speedup capacitor is not

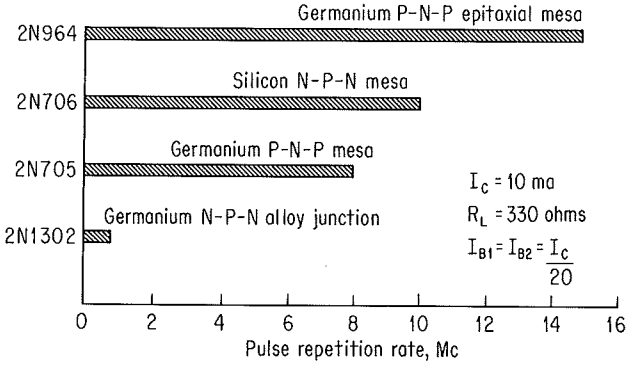


Fig. 6-21. Typical ranges of pulse repetition rate for various transistors.

connected to the circuit. Forward base current is 0.5 ma to give a forced current gain of 20. Reverse base current is equal to forward base current.

Upper limits of pulse repetition rate can be extended by any one of the following circuit modifications:

1. Increase forward and reverse base currents.
2. Decrease the collector load resistor.
3. Connect a speedup capacitor to the circuit.

6-9. LEAKAGE-CURRENT CONSIDERATIONS

Collector reverse (leakage) current is *always* present in a nonconducting transistor. The discussion of Sec. 1-8 indicated that this current is at a maximum when the base-emitter diode is open-circuited, is lowered as external base-emitter resistance is reduced, and is at a minimum when a reverse bias is applied to the base-emitter junction. Collector leakage current has the following detrimental effects:

1. Power is dissipated in the OFF-state transistor.
2. A substantial decrease in OFF-state collector voltage may occur as a result of voltage drop across the collector load resistor.
3. This leakage current, together with a base-emitter reverse-leakage current, may affect reverse-bias base-emitter voltage level of the OFF-state transistor.

Leakage current flows in a reverse-biased base-emitter diode. Application of a negative-voltage level to the base of a grounded-emitter N-P-N transistor causes base-emitter leakage current and collector leakage current to flow from the base terminal of the device. The combination of these two currents is the current I_{BX} described in Sec. 1-8. Current I_{BX} decreases reverse-bias base-emitter voltage level of the OFF-state transistor as shown in Fig. 6-22. Voltage drop across R_B causes $V_{BE(OFF)}$ to be less negative than applied voltage $-V$.

For circuit operation in which the header temperature does not rise appreciably above room temperature (25°C), most low- and medium-power transistors have sufficiently low values of collector leakage current and base-emitter leakage current for these parameters to be neglected in many circuit designs. However, collector leakage current *should* be considered in those circuits which fan out to more than one stage. Design of circuits having fan-out greater than unity is presented in Chap. 10; both collector leakage current and I_{BX} are considered in design of these circuits. Of the three examples of circuit design presented later in this chapter, one design example will apply to high-temperature operation of a transistor and will consider both collector leakage current and I_{BX}.

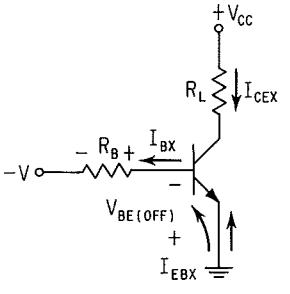


Fig. 6-22. Reduction of $V_{BE(OFF)}$ as a result of base leakage current.

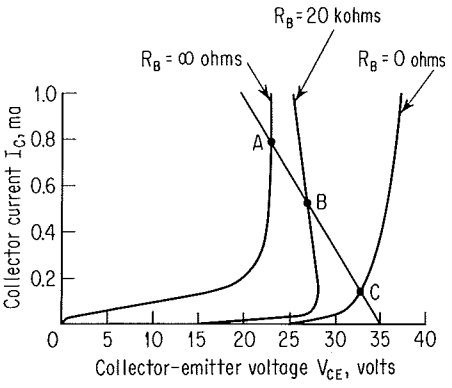


Fig. 6-23. Load line superimposed upon common-emitter collector characteristic curves in breakdown region.

6-10. SELECTION OF V_{CC}

In determining the maximum allowable value of V_{CC}, consideration must be given to the collector breakdown characteristics. Collector breakdown voltage of a common-emitter transistor stage may be at the $V_{(BR)CEO}$, $V_{(BR)CER}$, $V_{(BR)CES}$, or $V_{(BR)CEV}$ level, depending upon the input-circuit configuration. Figure 6-23 shows the plots of collector-emitter breakdown voltage given in Fig. 1-15, together with a possible load line for collector resistor R_L. Even though the base-emitter junction may not be forward-biased, collector current can be relatively large if V_{CC} is equal to 35 volts. For the given load line, an open-circuited base will cause the transistor to "latch up" at point A in the above figure; a 20-kilohm resistor from base to emitter terminals will reduce collector leakage current to the level at point B, and a short circuit from base to emitter will give the collector-current level of point C. The maximum allowable value of V_{CC} clearly depends upon the value of R_L and upon conditions existing at the base terminal during the OFF state of the transistor. For grounded-emitter operation of the transistor whose collector breakdown curves are given in Fig. 6-23, a collector supply voltage of 25 volts is sufficiently low, provided R_B is not greater than approximately 20 kilohms.

The lower limit of collector supply voltage is usually determined by allowable OFF-state collector voltage. If V_{CC} is low, NM_{ON} of the succeeding stage may be too low.

6-11. SELECTION OF LOAD RESISTOR

Equations for determining approximate fall time of a transistor switch were presented in Sec. 4-6. The derivation of these equations was based upon a value of collector load resistor R_L which was sufficiently small to have negligible effect upon charging rate of capacitance at the collector terminal. However, the effect of R_L may not always be negligible, especially when the transistor is a small-geometry mesa or planar device which turns off in only a few nanoseconds. Figure 6-24 shows a transistor inverter having external-load capacitance C_L. The figure also shows transistor internal capacitance C_{ob}. When the transistor is in saturation, the voltage level at point A is equal to $V_{CE(sat)}$: voltage across C_L has

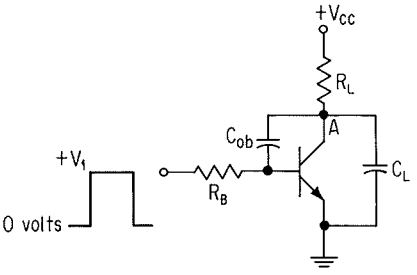


Fig. 6-24. Internal and external capacitive loading of inverter stage.

the $V_{CE(sat)}$ magnitude, while voltage across C_{ob} is equal to the difference between $V_{BE(ON)}$ and $V_{CE(sat)}$. After forward base drive is removed from the transistor and the device has just come out of saturation, the voltage level at point A begins to rise toward the V_{CC} value. Consider that decay time of the internal collector-current generator is negligibly small; fall time of the output signal is then determined by the rate at which C_{ob} and C_L charge through R_L. To a close approximation, $V_{CE(sat)}$ and $V_{BE(ON)}$ can be considered equal to zero volts. After the transistor has come out of saturation, voltage at point A can be described approximately by

$$V_A = V_{CC}(1 - e^{-t/R_L C_{eq}}) \tag{6-28}$$

where V_A = voltage at point A
C_{eq} = the sum of C_L and C_{ob}

From the above expression, voltage at point A is equal to $0.1V_{CC}$ at $t = 0.1R_LC_{eq}$ and is equal to $0.9V_{CC}$ at $t = 2.3R_LC_{eq}$. Thus, fall time of the output-voltage waveform can be written

$$t_f \approx 2.2R_LC_{eq} \tag{6-29}$$

For those circuits where t_f is a consideration, Eq. (6-29) can be used to calculate an approximate value for R_L. Actual fall time of the output-voltage waveform will be greater than that obtained from Eq. (6-29) because the transistor internal generator does not turn off instantaneously.

As pointed out in the discussion of Sec. 6-6, circuits of the class 1 type depend upon current through R_L to turn on a succeeding stage. Figure 6-14 shows that the load resistor of a class 1 circuit may be required to supply base current to one or more fan-out transistors. The value of R_L in a class 1 circuit is often determined by the amount of current which must be supplied through this resistor to an external load when the transistor is at cutoff.

Another consideration which may influence the value of R_L is the magnitude of collector cutoff current. The discussion of Sec. 6-9 pointed out that collector reverse current causes a voltage drop across R_L and reduces OFF-state collector voltage of the transistor. Too large a value of R_L may cause collector voltage of the nonconducting transistor to be below a desired level.

6-12. TYPICAL DESIGN ANALYSIS

As noted at the beginning of this chapter, it is not possible to give exact rules for inverter design. However, material presented thus far in the chapter can be

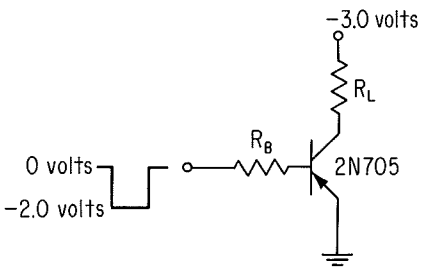


Fig. 6-25. Tentative circuit configuration for Example 6-1.

used as guidelines for suitable design. The following examples of circuit design are intended to illustrate typical design considerations.

EXAMPLE 6-1

PROBLEM: Design a saturated P-N-P inverter stage to be driven from a pulse generator. Rise and fall times of the pulse-generator waveform are each less than 20 nsec. Total switching time of the circuit is to be less than 300 nsec. Repetition rate of the circuit will not be greater than 2 Mhz. The following circuit parameters are given:

$V_{CC} = -3.0$ volts.
V_1 varies from 0 to -2.0 volts.

SOLUTION: *Step 1.* Figure 6-25 shows the tentative circuit configuration. A 2N705 germanium mesa transistor is selected on the basis of its relatively high-speed switching properties. A value of R_L is to be chosen, and R_B is to be selected to give a suitable value of forced gain. The circuit is then to be constructed and switching times measured. If switching response is too slow, one or more of the following may be done:

a. Add a speedup capacitor to the circuit.
b. Reduce the value of R_L.
c. Change the value of R_B.
d. Use a higher-speed transistor.

Step 2. Output capacitance of the device is approximately 5 pf. From Eq. (6-29), an R_L of 1.0 kilohm would, by itself, cause t_f to be no greater than 11 nsec. Since this time is small in comparison to the total switching time of 300 nsec, the 1.0-kilohm resistance value is selected for R_L.

Step 3. Measured common-emitter collector characteristic curves are shown in Fig. 6-26 for a 2N705 device. The curves show that for a collector current of 3.0 ma, h_{FE} is slightly less than 29 (determined at a V_{CE} of 0.4 volt). It would be desirable to use a large value of forward base current in order to turn the transistor on quickly. However, as there will be very little reverse base current, turnoff time of the device would probably be excessively large. Let forced current gain of the transistor be approximately 20. If saturated collector current were 3 ma, a forward base current of 0.15 ma would give a forced current gain of 20. Although collector current is slightly less than the 3-ma level, let forward base drive be equal to 0.15 ma.

Step 4. A portion of the 1.0-kilohm load line is superimposed upon the collector characteristic curves in Fig. 6-26. Collector saturation current is approximately 2.82 ma for a 0.15-ma base drive. A plot of V_{BE} versus I_C for a forward base current of 0.15 ma is given in Fig. 6-27. At a collector current of 2.82 ma, V_{BE} is approximately -0.326 volt. External base resistance can now be determined from Eq. (6-1) by substituting values of I_{B1}, V_1, and $V_{BE(ON)}$ into the expression; this yields

$$R_B = \frac{2.0 - 0.326}{0.15} = 11.15 \text{ kilohms}$$

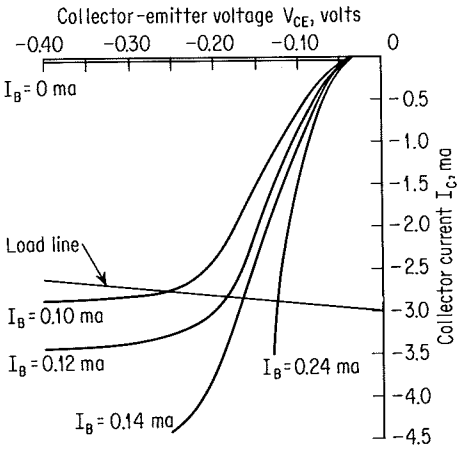


Fig. 6-26. Common-emitter collector characteristics for 2N705 transistor.

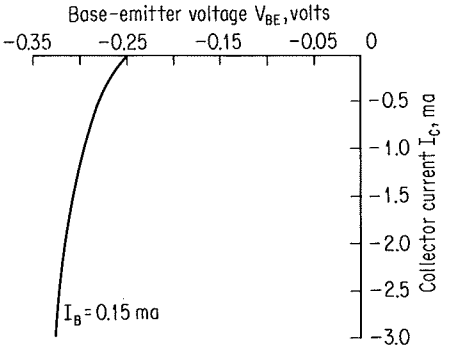


Fig. 6-27. Base-emitter voltage versus collector current for forward base current of 0.15 ma (2N705).

Resistors are generally available in certain discrete values. A standard 11.0-kilohm resistor is chosen for R_B. This resistance value increases I_{B1} to approximately 0.152 ma.

Step 5. The circuit shown in Fig. 6-25 was fabricated; R_L and R_B had values of 1.0 and 11.0 kilohms, respectively. Measured switching times of the circuit, in nanoseconds, are given below.

t_d	t_r	t_s	t_f
40	300	30	225

Total switching time of the circuit is above the 300-nsec time limit. A speedup capacitor of 18 pf connected across R_B gives the following switching times in nanoseconds:

t_d	t_r	t_s	t_f
6	7	6	36

The circuit now switches sufficiently fast.

Step 6. It has not yet been determined whether recovery time of the speedup capacitor will allow the 2-Mhz pulse repetition rate. Observation of the base-voltage waveform reveals that base voltage decreases from the reverse-bias positive level to zero volts in approximately 50 nsec. The inverter stage is able to operate at a 2-Mhz pulse repetition rate.

EXAMPLE 6-2

PROBLEM: Design a saturated P-N-P inverter stage in which a bias supply is used to provide reverse base drive. A speedup capacitor is not to be used in the circuit. Circuit parameters are as given in Example 6-1. Switching-speed requirements of the above example are to be met; the same pulse generator is to drive the present stage.

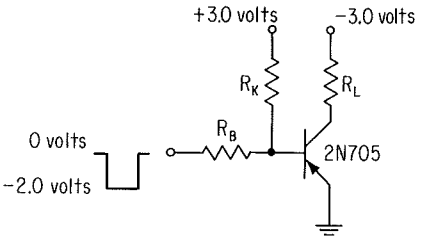


Fig. 6-28. Circuit configuration for Example 6-2.

SOLUTION: *Step 1.* Figure 6-28 shows the circuit configuration. The positive voltage supply is arbitrarily selected to be 3.0 volts. The same 2N705 transistor of Example 6-1 is to be used in the present circuit. A value of 1.0 kilohm is chosen for R_L. From the previous example, it is known that a forward base current of 0.15 ma is too low to turn on the transistor quickly. As a start, select a value of 0.3 ma for forward base drive. If this current level proves to be too low, the circuit can be redesigned for a larger base-drive current.

Step 2. Let reverse base current equal the magnitude of forward base current.

Step 3. Equations (6-8) and (6-9) can be combined to give

$$I_{B1} + I_{B2} = \frac{V_1}{R_B} \tag{6-30}$$

Values of I_{B1}, I_{B2}, and V_1 are substituted into the above expression to yield

$$R_B = 3.33 \text{ kilohms}$$

Step 4. Equation (6-18) can now be solved for R_K to give

$$R_K = 16.4 \text{ kilohms}$$

Step 5. If the value of $V_{BE(\text{OFF})}$ is desired, Eq. (6-11) can be used to give

$$V_{BE(\text{OFF})} = 0.507 \text{ volt}$$

This magnitude of base-emitter reverse voltage is well below the $V_{(BR)EBO}$ rating of the transistor.

As an independent check upon the calculated values of R_B and R_K, a Thévenin equivalent circuit can be used to determine values of I_{B1} and I_{B2}. Figure 6-29 shows the above circuit disconnected at points AA'; calculated values of R_B and R_K are also shown. For a −2.0-volt input signal, voltage at point A is −1.155 volts. The equivalent resistance R_T seen to the left at point A is the parallel combination of R_B and R_K, or 2.77 kilohms. Figure 6-30 shows the Thévenin equivalent circuit connected to the transistor base. The input signal to R_T varies

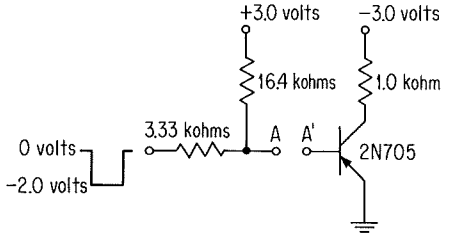


Fig. 6-29. Circuit of Fig. 6-28 disconnected at points AA'.

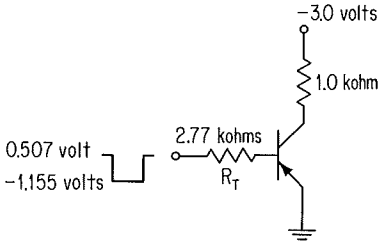


Fig. 6-30. Circuit of Fig. 6-29 with Thévenin equivalent input circuit.

between 0.507 and −1.155 volts. Substitution of R_T for R_B in Eqs. (6-1) and (6-2) gives values for I_{B1} and I_{B2}, repectively. From Eq. (6-1),

$$I_{B1} = \frac{1.155 - 0.326}{2.77} = 0.3 \text{ ma}$$

and from Eq. (6-2),

$$I_{B2} = \frac{0.507 - 0.326}{2.77} = 0.3 \text{ ma}$$

The above calculations show that resistance values for R_B and R_K give the desired base-drive currents.

Step 6. The circuit of Fig. 6-28 was fabricated with the following resistance values:

$R_L = 1.0$ kilohm
$R_B = 3.3$ kilohms
$R_K = 16.0$ kilohms

Measured switching times of the circuit, in nanoseconds, are:

t_d	t_r	t_s	t_f
40	84	30	68

Total switching time of the circuit is less than the 300-nsec maximum specification.

EXAMPLE 6-3

PROBLEM: Design a circuit of the type given in Fig. 6-31 to operate at a temperature of 100°C. Switching speed of the circuit is not important. Use N-P-N silicon transistors which have the following characteristics at 100°C:

Parameter	Test conditions	Value
I_{CEX}	$V_{BE} = -0.5$ volt $V_{CE} = 6.0$ volts	50 μa
I_{BX}	$V_{BE} = -0.5$ volt	55 μa
h_{FE}	$I_C = 0.6$ ma $V_{CE} = 1.0$ volt	40
$V_{CE(\text{sat})}$	$I_C = 0.6$ ma $I_B = 0.03$ ma	0.3 volt
$V_{BE(\text{ON})}$	$I_C = 0.6$ ma $I_B = 0.03$ ma	0.6 volt

Parameters h_{FE}, $V_{CE(\text{sat})}$, and $V_{BE(\text{ON})}$ are given at an I_C level of 0.6 ma in order that an R_L of 10 kilohms can be used in the design. The large value of R_L is selected to accentuate the effects of collector leakage current.

SOLUTION: The design analysis will proceed to determine values for the two unknown circuit parameters R_B and R_K. These two resistors are to be selected to provide a suitable forward base drive as well as a reverse-bias voltage level of −0.5 volt. (This value of $V_{BE(\text{OFF})}$ is chosen in order to use given values of I_{CEX} and I_{BX}.)

Step 1. Figure 6-32 shows the input-circuit to transistor Q_2 for transistor Q_1 at cutoff.

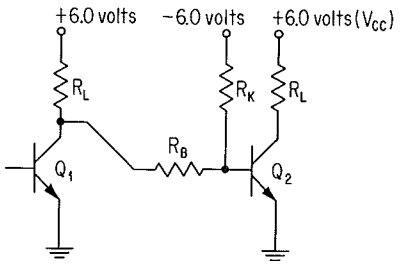


Fig. 6-31. Circuit configuration for Example 6-3.

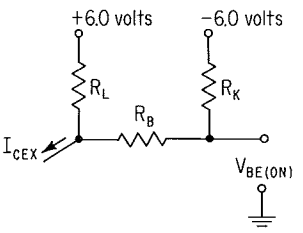


Fig. 6-32. Input circuit to Q_2 of Fig. 6-31 for Q_1 at cutoff.

Voltage drop across R_L as a result of leakage current I_{CEX} effectively reduces magnitude of the +6.0-volt supply. Figure 6-33 shows an equivalent circuit of the above network. Voltage V' is determined to be

$$V' = 6.0 - I_{CEX}R_L = 5.5 \text{ volts}$$

From Fig. 6-33,

$$I_{B1} = I_1 - I_2 \tag{6-31}$$

$$I_1 = \frac{V' - V_{BE(ON)}}{R_L + R_B} \tag{6-32}$$

$$I_2 = \frac{V_{BB} + V_{BE(ON)}}{R_K} \tag{6-33}$$

Substitution of Eqs. (6-32) and (6-33) into Eq. (6-31) yields

$$I_{B1} = \frac{V' - V_{BE(ON)}}{R_L + R_B} - \frac{V_{BB} + V_{BE(ON)}}{R_K} \tag{6-34}$$

Equation (6-34) is similar to Eq. (6-19), except that collector leakage current is now considered. For adequate forward base drive,

$$I_{B1} > \frac{I_C}{h_{FE}} \tag{6-35}$$

Let

$$I_{B1} = \frac{2I_C}{h_{FE}} \tag{6-36}$$

(This will give a value of approximately 0.03 ma for I_{B1} and allows given values of $V_{CE(sat)}$ and $V_{BE(ON)}$ to be used in later calculations.) An expression can be written for I_C which, when

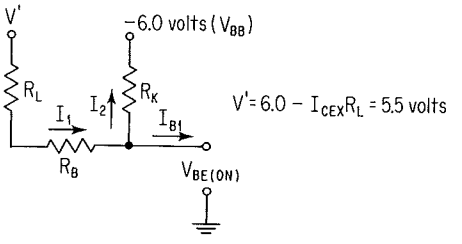


Fig. 6-33. Equivalent-circuit representation of circuit in Fig. 6-32.

substituted into Eq. (6-36), gives

$$I_{B1} = \frac{2(V_{CC} - V_{CE(\text{sat})})}{h_{FE}R_L} \tag{6-37}$$

Equating the right sides of Eqs. (6-34) and (6-37) yields

$$\frac{2(V_{CC} - V_{CE(\text{sat})})}{h_{FE}R_L} = \frac{V' - V_{BE(\text{ON})}}{R_L + R_B} - \frac{V_{BB} + V_{BE(\text{ON})}}{R_K} \tag{6-38}$$

The above expression can be solved for R_K to give

$$R_K = \frac{V_{BB} + V_{BE(\text{ON})}}{(V' - V_{BE(\text{ON})})/(R_L + R_B) - 2(V_{CC} - V_{CE(\text{sat})})/h_{FE}R_L} \tag{6-39}$$

Equation (6-39) contains only two unknown circuit parameters R_K and R_B. This expression is derived for Q_2 in saturation and is referred to as the ON equation. Various values of R_B can be substituted into the above expression, together with known values of all other parameters on the right side of the equation, to yield values of R_K. Corresponding values of R_B and R_K give a 0.03-ma forward base drive to Q_2 when Q_1 is at cutoff.

Step 2. Figure 6-34 shows conditions existing at the base of Q_2 when Q_1 is in saturation. An equation can be written for base-emitter reverse-bias voltage in terms of V_{BB}, $V_{CE(\text{sat})}$, R_B, R_K, and I_{BX}. This equation can be solved for R_K to yield

$$R_K = \frac{V_{BB} - V_{BE(\text{OFF})}}{(V_{CE(\text{sat})} + V_{BE(\text{OFF})})/R_B + I_{BX}} \tag{6-40}$$

Equation (6-40) is valid for Q_2 at cutoff and is referred to as the OFF equation. Calculated values of R_K, together with corresponding values of R_B, give a -0.5-volt bias to the base of Q_2 when Q_1 is in saturation.

Step 3. Figure 6-35 shows plots of the ON and OFF equations. The two curves are seen to intersect at points A and B. Thus, there are two combinations of R_K and R_B which will give the desired forward base current and reverse-bias voltage.

DISCUSSION: The question arises as to whether resistances R_K and R_B should be selected to have the values at point A or at point B. Reverse-bias voltage and forward base current to the transistor are identical for either of the two combinations of resistance values. For resistance values at point A, reverse base drive is determined to be 0.41 ma, whereas only 0.11 ma of reverse base drive is calculated if R_K and R_B have the values at point B. Consequently, the circuit will turn off more quickly if R_K and R_B have the values at point A. However, if R_K and R_B are selected to have the values at point B, less current flows through these two resistors when Q_2 is at cutoff; standby-power dissipation of the circuit is now reduced.

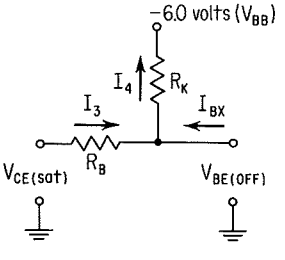


Fig. 6-34. Input-circuit conditions for Q_2 of Fig. 6-31 when Q_1 is saturated.

For any value of R_B, a value of R_K larger than that calculated from Eq. (6-39) will give a greater forward base drive than the minimum required value determined from Eq. (6-36). A smaller value of R_K than that calculated from Eq. (6-40) will cause an even more negative reverse-bias voltage to appear at the base of Q_2. In order to obtain at least the minimum required forward base drive and also a $V_{BE(\text{OFF})}$ level at least as negative as -0.5 volt, R_K cannot lie above the OFF equation plot, nor can it lie below the ON equation plot. Thus, the common area between the curves of Fig. 6-35 is an *area of solution* for the circuit under discussion.

In order to assure that the circuit will continue to operate for slight variations of transistor parameters, resistor values, or

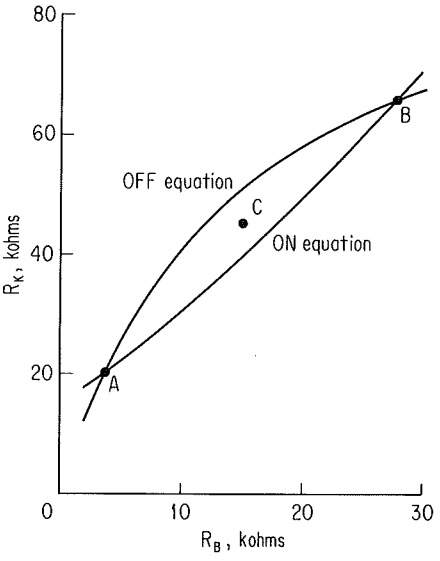


Fig. 6-35. Plots of ON and OFF equations for circuit of Example 6-3.

supply-voltage magnitudes, it is convenient to choose values of R_B and R_K which lie safely within the above area of solution. Point C of Fig. 6-35 depicts a suitable choice for R_B and R_K; these values of resistance give the following circuit parameters:

$$I_{B1} = 0.05 \text{ ma}$$
$$V_{BE(\text{OFF})} = -1.12 \text{ volts}$$
$$I_{B2} = 0.15 \text{ ma}$$

7

Graphical Circuit Analysis

7-1. INTRODUCTION

The discussion of Sec. 1-7 pointed out that a nonlinear relationship exists between base-emitter voltage drop of a transistor and currents flowing in the device. This was illustrated by the plot of Fig. 1-7. Similar curves are shown in Fig. 7-1 for a 2N3832 transistor; voltage drop is shown as V_{BE} and is identical to the term $V_{BE(ON)}$ referred to in previous discussions. In order to simplify the calculation of base current, many design analyses consider that V_{BE} has a constant value for the particular device. This technique allows rapid calculation of base currents and, since the assumed values of V_{BE} are reasonably close to the actual values, provides answers which are approximately correct. A base current calculated in the above manner can be projected onto a curve of the type shown in Fig. 7-1 and a corresponding value of V_{BE} obtained. If the assumed V_{BE} level is not equal to the value obtained from the curve, the above procedure can be repeated for a second assumed value of V_{BE}. Repetition of this process will eventually yield actual circuit values of I_B and V_{BE}.

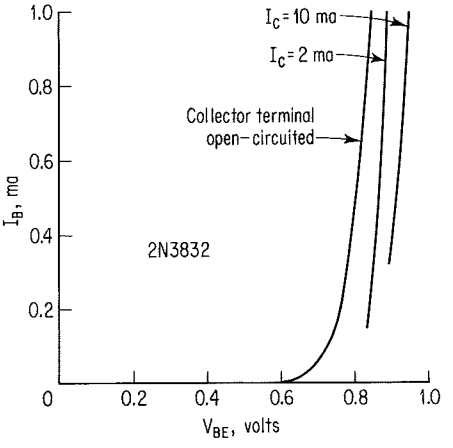


Fig. 7-1. Effects of collector current and base current upon base-emitter voltage.

Graphical techniques can be used to obtain exact values of currents and voltages in a transistor circuit. In addition, a graphical analysis quickly shows effects of various circuit parameters upon dc current and voltage levels. Previous discussions have already illustrated use of a load line to obtain I_C and V_{CE}. The object of this chapter is to describe graphical techniques for determining I_B, V_{BE}, and I_E. This material is useful for saturated-inverter design and will provide a background for later analysis of the emitter-follower and current-mode switching circuits.

7-2. LINEAR CIRCUIT CONSIDERATIONS

Graphical analysis involves plots of current and voltage levels associated with the various circuit elements. Consider the resistor circuit shown in Fig. 7-2*a*. The positive direction of voltage is defined as a *rise* from terminals B to A; positive current flow is defined as a current flow *into* terminal A. The current-voltage characteristic of the resistor is given in Fig. 7-2*b*. This plot is determined by assuming an applied voltage across the resistor and calculating the current which flows for each value of voltage. The resulting characteristic is a straight line of slope $1/R$ which passes through the origin. Negative values of currents and voltages are also included in the plot, as a negative-voltage level at terminal A (with respect to terminal B) will give a negative-current level. The straight-line VI plot is a result of the linear relationship between current through a resistor and the corresponding voltage across the resistor. If an actual voltage source is applied across the resistor, the above VI plot shows the resulting current flow. Thus, for an applied voltage of magnitude V', current through the resistor (and through the voltage source) has the value I'.

Individual VI characteristics can be obtained for various circuit elements and combined to form a composite VI plot for all elements of a circuit. Figure 7-3*b* shows individual VI plots for series-connected resistors R_1 and R_2 of Fig. 7-3*a*. Each plot is obtained in the same manner as before, with various assumed voltage levels applied to the individual resistors. A plot of current and voltage levels at terminals A and B is generally of more concern than the individual VI plots for R_1 and R_2. If a voltage is applied across the series combination of R_1 and R_2, the same current must flow through the two resistors, and the sum of the voltage drops across the two resistors must equal the applied voltage. The VI plots for series-

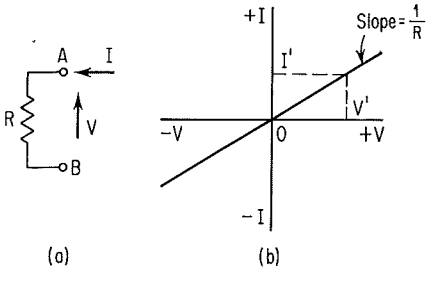


Fig. 7-2. Single-resistor circuit and VI plot.

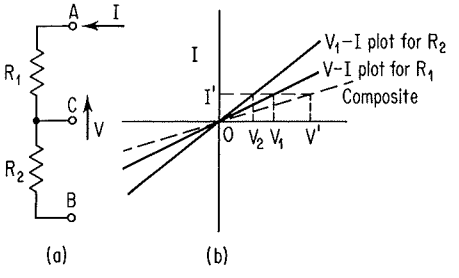


Fig. 7-3. Series-resistor circuit and VI plots.

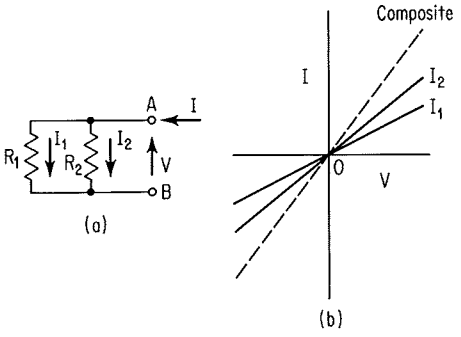


Fig. 7-4. Parallel-resistor circuit and *VI* plots.

connected resistors can be obtained by adding voltage drops across the resistors for constant levels of current. A composite curve for resistors R_1 and R_2 in series is also shown in Fig. 7-3*b*. For an applied voltage V' across the two resistors in series, current through the resistors has the magnitude I'; voltages across R_1 and R_2 are determined from the individual *VI* characteristics to be V_1 and V_2, respectively.

Figure 7-4*a* shows a circuit consisting of parallel resistors R_1 and R_2. Current I into terminal A is equal to the sum of currents I_1 and I_2. Figure 7-4*b* shows individual *VI* plots for the two resistors, as well as the composite *VI* characteristic for the circuit. The composite *VI* plot is obtained by adding I_1 and I_2 for various constant values of V.

Consider next the circuit shown in Fig. 7-5*a*. The composite *VI* plot for this circuit can be determined, as before, by calculating current flow at terminal A for various values of assumed voltage across terminals A and B. For a short-circuit connection across the terminals, current has the value V_1/R_1. Since positive current flow is defined to be *out* of terminal A, the above current level is plotted in Fig. 7-5*b* as a *positive* value at an applied voltage level of zero volts. For a positive applied voltage equal to the magnitude of V_1, there is no current flow through the circuit, and the *VI* plot crosses the current axis at a voltage level of V_1 as shown. The above two plotted points lie along the straight-line *VI* plot of the circuit. Figure 7-5*c* illustrates another method of obtaining a composite *VI* plot for the circuit. Individual *VI* curves are plotted for the resistor and voltage source. The resistor alone has a *VI* plot of negative slope which passes through the origin. The voltage source has a *VI* characteristic which is a locus of constant voltage. Since the resistor and voltage source are in series, the individual *VI* plots for the

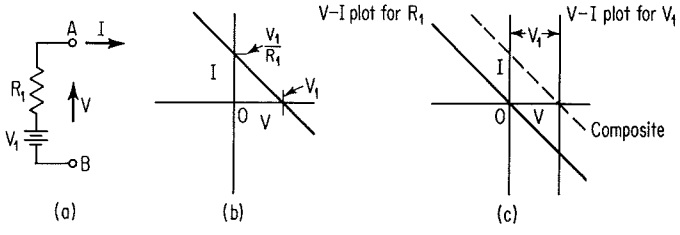


Fig. 7-5. Voltage source and resistance, together with *VI* plots.

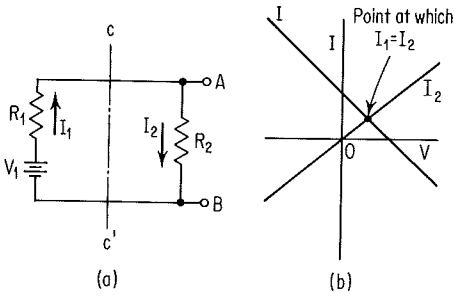


Fig. 7-6. Voltage source and two series resistances analyzed as a two-branch network.

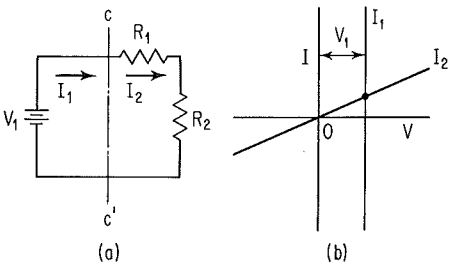


Fig. 7-7. Alternate method for analyzing voltage source and two series resistances as a two-branch network.

two elements can be added at various constant-current levels to obtain the composite *VI* plot for the circuit. This composite plot is seen to be identical to the one obtained in Fig. 7-5*b*.

Figure 7-6*a* shows resistor R_2 connected across terminals *A* and *B* of the previous circuit. Voltage across *AB* and current flow in the circuit can be determined in the following manner. If the circuit is considered to be split into two branches by the line *cc'*, separate *VI* plots can be obtained for the left and right branches. These two plots are shown in Fig. 7-6*b*. For the two branches connected together, currents I_1 and I_2 are equal; in addition, the same voltage appears across the two branches. The above conditions exist only at the intersection of the *VI* plots for the separate branches; this point of intersection determines current level in the circuit and also the voltage across *AB*.

The above circuit can also be analyzed as shown in Fig. 7-7*a* and *b*. In Fig. 7-7*a* the circuit is divided into two branches; one branch contains the voltage source V_1 and the other branch contains resistors R_1 and R_2 in series. Figure 7-7*b* shows *VI* plots for each of these branches. Current magnitude in the circuit is determined from the point of intersection of the two plots.

7-3. NONLINEAR *VI* PLOTS—DIODE CHARACTERISTICS

Diodes are nonlinear circuit elements which conduct a small (reverse-leakage) current when reverse-biased and a relatively large current when sufficiently forward-biased. Figure 7-8 shows four diode circuits, together with a corresponding *VI* plot for each circuit. Each of the plots shows the familiar diode characteristic curve located in a different quadrant of the *VI* plane. This is a result of the particular circuit connection, together with defined directions of positive voltage and current levels. In Fig. 7-8*a*, positive current is defined to flow *into* the diode. As applied voltage increases in a positive sense beyond the diode-conduction threshold, current flows in the positive direction through the diode. The *VI* plot in Fig. 7-8*b* shows that positive current is associated with a positive voltage. Negative values of voltage are seen to give a zero-level current.* If

* Diode reverse-leakage current is small and is neglected in the various *VI* plots of Fig. 7-8.

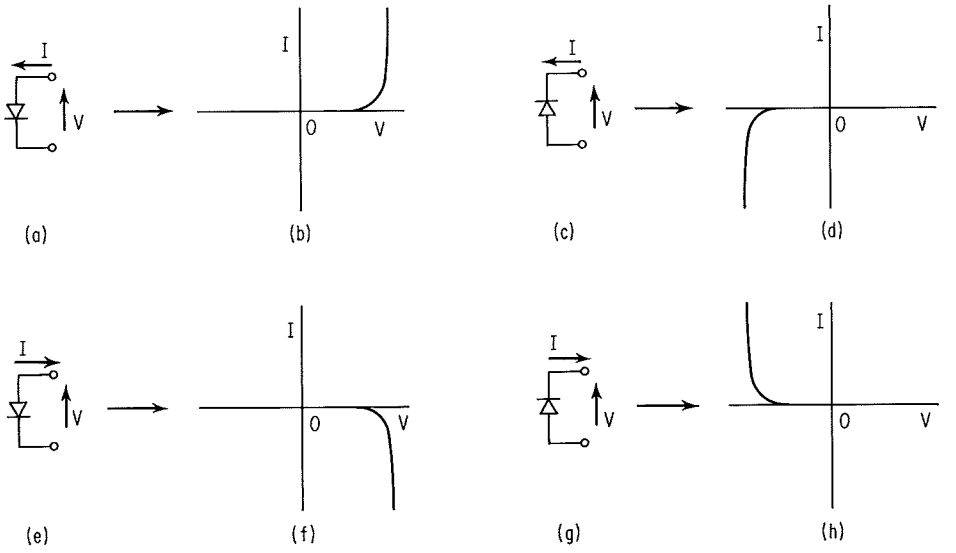


Fig. 7-8. Various combinations of diode connections and defined positive directions for currents and voltages, together with resulting *VI* plots.

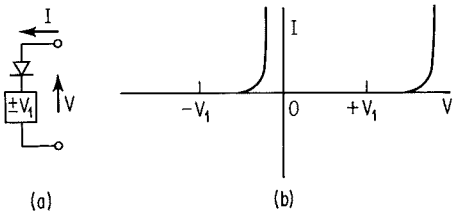


Fig. 7-9. Series connection of voltage source and diode, together with resulting *VI* plots.

voltage in Fig. 7-8*c* is made increasingly positive (but less positive than the reverse-breakdown voltage), positive current does not flow in the circuit. A negative level of applied voltage will allow diode current to flow, but the direction of current flow will be *opposite* to the defined positive direction. Thus, a *negative* current flows for a *negative* voltage; the plot of Fig. 7-8*d* shows the resulting *VI* characteristic of this particular circuit. The remaining two circuits (Fig. 7-8*e* and *g*) can readily be analyzed to obtain the corresponding *VI* plots.

A voltage source in series with a diode causes a shift in the diode characteristic curve. This is illustrated in Fig. 7-9 for positive and negative polarities of series voltage.

7-4. NETWORKS OF RESISTORS AND DIODES

Resistor and diode *VI* curves can be combined graphically, by the methods described above for combining resistor *VI* plots, to yield composite *VI* plots. Figure 7-10*a* shows a resistor and diode connected in series. In Fig. 7-10*b* individual plots are given for the two circuit elements; a composite *VI* plot of the

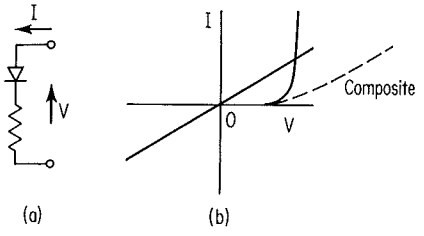


Fig. 7-10. Series connection of resistor and diode, together with resulting *VI* plots.

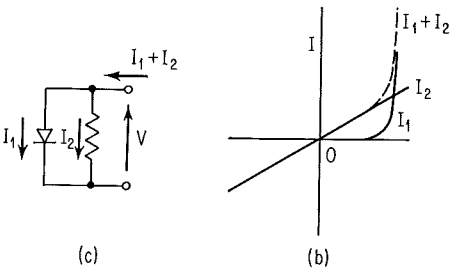


Fig. 7-11. Parallel connection of resistor and diode, together with resulting *VI* plots.

circuit is also shown. Figure 7-11*a* shows a parallel connection of a diode and a resistor. Individual *VI* plots, as well as the composite *VI* plot of the circuit, are given in Fig. 7-11*b*.

7-5. TRANSISTOR INPUT CHARACTERISTICS

Base-emitter voltage drop of a transistor can be expressed graphically as shown in Fig. 7-12. This plot gives the relation between voltage across the base-emitter diode and emitter current of the transistor. Collector-emitter voltage of the transistor has a slight effect upon the magnitude of V_{BE}. At larger levels of V_{CE}, base width narrows, and the emitter injects a greater number of carriers into the base region;[1] this increases I_E, although V_{BE} remains constant. Thus, for the same level of I_E, the V_{BE} drop is lower for increased values of V_{CE}. Measured plots of I_E versus V_{BE} for a 2N3832 transistor, at two different levels of V_{CE}, are given in Fig. 7-13. The figure shows that as V_{CE} is made larger, the same I_E level can be maintained at a lower value of V_{BE}.

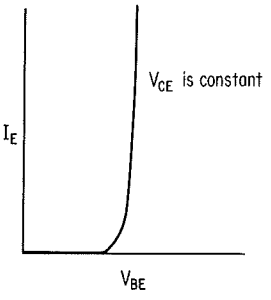


Fig. 7-12. Graphical relationship between emitter current and base-emitter voltage.

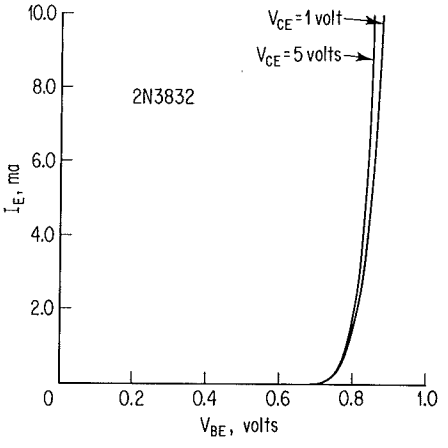


Fig. 7-13. Relationship between emitter current, base-emitter voltage, and collector-emitter voltage.

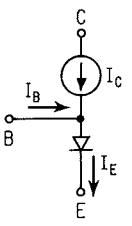


Fig. 7-14. Simplified equivalent circuit of transistor.

Figure 7-14 shows a transistor equivalent circuit which is useful for the present discussion. Base current I_B and collector current I_C flow through the base-emitter diode. As base current of the transistor is a terminal current of the base-emitter diode, it is possible to show a plot of the relation between I_B and V_{BE}. If the transistor is not saturated, $I_C = \alpha I_E$, and

$$I_B = \frac{I_E}{h_{FE} + 1} \tag{7-1}$$

Plots of I_B versus V_{BE} can be obtained by suitably scaling the vertical axis of the I_E versus V_{BE} plots of Fig. 7-13. Care must be exercised to assure that the correct value of h_{FE} is used during the above process of changing the I_E axis to an I_B axis. Figure 7-15 gives measured plots of I_B versus V_{BE} for the 2N3832 device at the same two values of V_{CE} used in Fig. 7-13. Figure 7-15 shows that for the particular 2N3832 device, an increase in V_{CE} causes a decrease in V_{BE} for a constant level of I_B.

Equation (7-1) is not valid for a saturated transistor because $I_C < \alpha I_E$. Collector current is limited by series resistance in the collector circuit and may have a constant value (or nearly so) over a wide range of base currents. Measured plots showing I_B versus V_{BE} at various constant values of I_C are given in Fig. 7-1 for a 2N3832 transistor.

7-6. INPUT CURRENT AND VOLTAGE LEVELS FOR THE SATURATED INVERTER

Nonlinear VI plots for the base-emitter diode of a transistor can be graphically combined with VI characteristics of linear elements in order to obtain base and emitter currents of the transistor. This section describes a graphical analysis for the saturated common-emitter stage. Nonsaturated-transistor operation is graphically analyzed in Chaps. 8 and 11.

Two examples are presented below which show typical input-circuit designs.

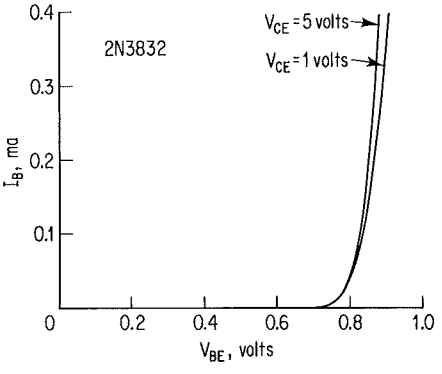


Fig. 7-15. Relationship between base current, base-emitter voltage, and collector-emitter voltage.

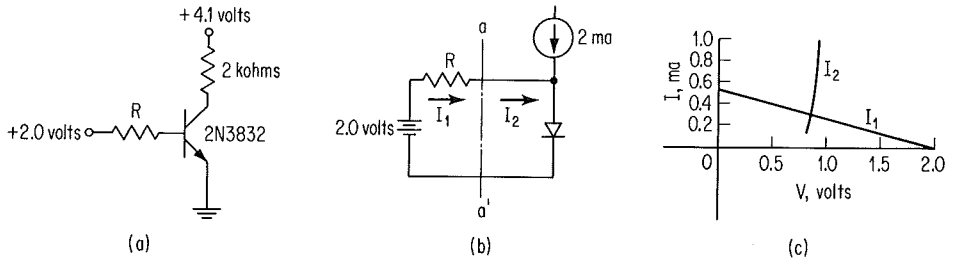


Fig. 7-16. Graphical analysis to determine base series resistance for a specified forward base current.

The transistor type is a 2N3832. The nonlinear *VI* input characteristic used in each example is obtained from the plots of Fig. 7-1.

EXAMPLE 7-1

PROBLEM: The grounded-emitter stage of Fig. 7-16*a* conducts 2 ma of collector current when the transistor is saturated. Determine the value of R which will provide a forward base drive of 0.3 ma.

SOLUTION: Figure 7-16*b* shows an equivalent-circuit representation of the input portion of the transistor circuit. The equivalent circuit is divided into two branches by the line *aa'*.

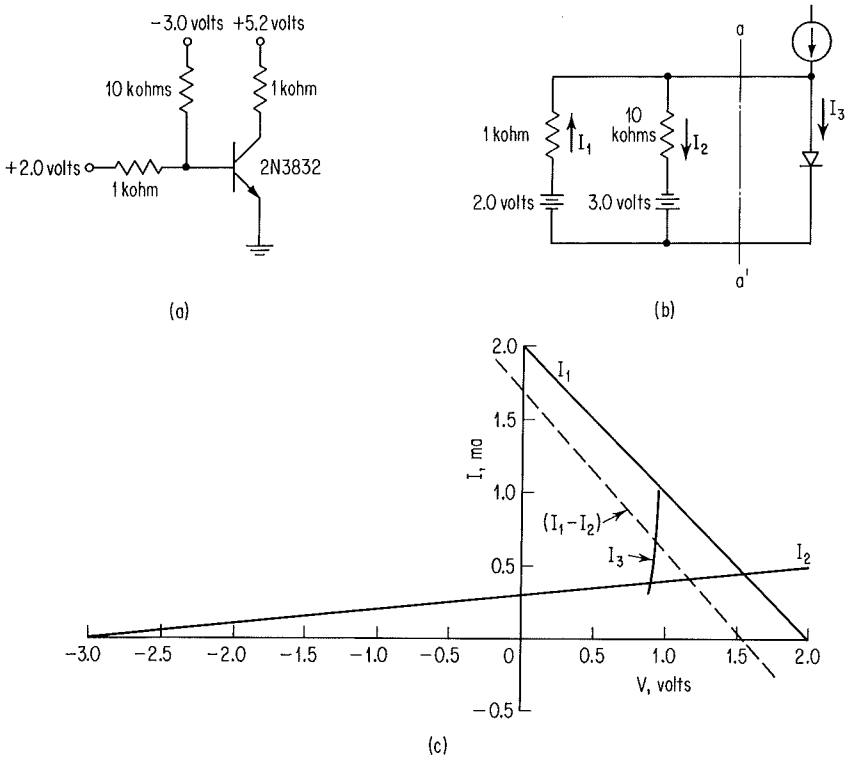


Fig. 7-17. Graphical analysis to determine forward base current and base-emitter voltage.

Table 7-1. Graphical and Measured Values of I_{B1} and V_{BE} for Circuit of Fig. 7-17a

Parameter	Graphical value	Measured value
I_B	0.68 ma	0.69 ma
V_{BE}	0.93 volt	0.92 volt

Figure 7-16*c* shows a *VI* plot of the diode characteristic, together with a *VI* plot of the voltage source in series with R. The slope of R has been selected such that the two *VI* plots intersect at an I_B of 0.3 ma. The required value of R is graphically determined to be 4.45 kilohms.

EXAMPLE 7-2

PROBLEM: Determine forward base current and base voltage for the circuit shown in Fig. 7-17*a*.

SOLUTION: *Step 1.* If base current is sufficiently large, the transistor will saturate, and collector current will be at a level of 10 ma. For an assumed $V_{BE(ON)}$ of 0.9 volt, a calculation of I_{B1}, by the method described in Sec. 6-2, yields a value of 0.71 ma. The I_B versus V_{BE} plots of Fig. 7-1 show that the transistor can conduct 10 ma of collector current at a forward base current of 0.71 ma.

Step 2. An equivalent input-circuit configuration is shown in Fig. 7-17*b*; the circuit is divided into two parts by the line *aa'*. Individual *VI* plots for I_1, I_2, and I_3 are given in Fig. 7-17*c*. The equivalent-circuit configuration shows that I_3 is equal to $I_1 - I_2$. A *VI* plot of $I_1 - I_2$ is shown in Fig. 7-17*c*. The point of intersection of this composite plot and the diode plot shows levels for base current and base-emitter voltage of the transistor; base current is determined to have a value of 0.68 ma, and base-emitter voltage is at a level of 0.93 volt.

DISCUSSION: The circuit of Fig. 7-17*a* was breadboarded. Table 7-1 gives a comparison of graphical values and measured values of forward base current and base-emitter voltage. This method of circuit analysis graphically shows the effects of varying input voltages and input resistors. If either of the two input voltage levels is varied, the resulting composite curve of Fig. 7-17*c* shifts position but remains parallel to the original composite curve. Position and slope of the composite plot are changed if either of the two input resistors is varied.

REFERENCE

1. Early, J. M.: Effects of Space-charge Layer Widening in Junction Transistors, *Proc. IRE,* vol. 40, p. 1401, November, 1952.

8

Emitter-follower Operation and Design

8-1. PRINCIPLES OF OPERATION

It will be recalled from the discussion of Sec. 4-2 that a transistor may be connected in the common-collector configuration, with input and output signals appearing at base and emitter terminals, respectively. This type of circuit is often referred to as an "emitter-follower circuit." Figure 8-1 shows a transistor connected in the emitter-follower configuration. Although the collector terminal is at $+V_{CC}$ volts, it is shorted to ground for ac signals; the transistor is connected as a common-collector circuit element.

Base current flows into the transistor of Fig. 8-1 when a positive-input signal rises above the base-emitter turn-on voltage level. The potential difference across base and emitter terminals is equal to the value of $V_{BE(ON)}$. Thus, the output potential is slightly less positive than the input-voltage level and follows closely the voltage excursion of the positive-input signal. Voltage gain of the circuit is given by

$$A_V = \frac{V_{in} - V_{BE(ON)}}{V_{in}} \tag{8-1}$$

where A_V = voltage gain of the emitter-follower circuit
V_{in} = dc level of input signal

The above expression approaches unity for $V_{in} \gg V_{BE(ON)}$.

The maximum positive-voltage level at the base terminal is limited by the value of V_{CC} and the turn-on voltage of the base-collector diode. If base-terminal voltage rises to a level which causes the base-collector diode to conduct, a clamping action occurs which will not allow the base voltage to become significantly more positive. This clamped-voltage level is the sum of V_{CC} and the magnitude of base-collector diode drop. In order to prevent clamping of the input-signal level, V_{CC} should be at least as positive as the most positive input-voltage level.

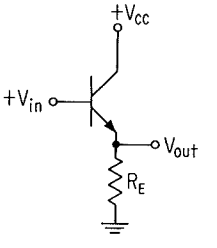


Fig. 8-1. Emitter-follower configuration.

Collector current of the nonsaturated transistor is given by

$$I_C = h_{FE} I_B \tag{8-2}$$

Emitter current is expressed by

$$I_E = I_C + I_B \tag{8-3}$$

Substitution of the right side of Eq. (8-2) for I_C in Eq. (8-3) yields

$$I_E = I_B(h_{FE} + 1) \tag{8-4}$$

Current gain is defined to be the ratio of input current to output current and, from Eq. (8-4), can be expressed

$$A_I = \frac{I_E}{I_B} = h_{FE} + 1 \tag{8-5}$$

8-2. CIRCUIT CHARACTERISTICS

Input impedance of the emitter-follower circuit is affected by current gain of the transistor and by magnitude of the emitter load impedance. A dc and an ac input impedance exist for the emitter-follower circuit. The dc input impedance is defined by

$$R_{\text{in}} = \frac{V_{\text{in}}}{I_B} \tag{8-6}$$

If the circuit has no external series base resistance, V_{in} appears at the base terminal and can be written

$$V_{\text{in}} = V_E + V_{BE(\text{ON})} \tag{8-7}$$

where V_E is the voltage at the emitter terminal. Voltage V_E is related to I_E and R_E in the following manner

$$V_E = I_E R_E \tag{8-8}$$

The right side of Eq. (8-8) can be substituted for the V_E term in Eq. (8-7) to give

$$V_{\text{in}} = I_E R_E + V_{BE(\text{ON})} \tag{8-9}$$

From Eq. (8-4)

$$I_B = \frac{I_E}{h_{FE} + 1} \tag{8-10}$$

Substitution of the right side of Eqs. (8-9) and (8-10) into Eq. (8-6) gives, after slight manipulation of terms,

$$R_{\text{in}} = R_E(h_{FE} + 1) + \frac{V_{BE(\text{ON})}(h_{FE} + 1)}{I_E} \tag{8-11}$$

For I_E larger than 2 or 3 ma,

$$R_{\text{in}} \approx R_E(h_{FE} + 1) \tag{8-12}$$

This expression shows that dc input resistance of the emitter-follower stage is approximately equal to $h_{FE} + 1$ times the emitter load resistance.

Small-signal, or ac, input impedance is a complex quantity which depends upon frequency of the input signal. At low frequencies, this impedance can be expressed[1]

$$Z_i = \frac{v_i}{i_b} = r_b' + (r_e + Z_E)(h_{fe} + 1) \tag{8-13}$$

where Z_i = ac input impedance
v_i = incremental change in input voltage
i_b = incremental change in base current
Z_E = external impedance at the emitter terminal

Typically, $r_b' \ll (r_e + Z_E)(h_{fe} + 1)$. In addition, $h_{fe} \approx h_{FE}$. For current levels at which $r_e \ll R_E$, low-frequency ac input impedance of the emitter-follower circuit is given approximately by

$$Z_i \approx Z_E(h_{FE} + 1) \tag{8-14}$$

The emitter-follower stage acts as an impedance transformer from output to input terminals and is often used as a buffer element between an inverter stage and an external load. This application of the emitter-follower circuit is illustrated by the diagrams of Fig. 8-2. An external load connected to an inverter circuit is shown in Fig. 8-2*a*. The load, consisting of resistance R_T and capacitance C_T, represents a common form of impedance encountered in transistor circuitry. Consider that the above inverter stage is turned on; the transistor is in saturation, and voltage across the resistor-capacitor combination has the value $V_{CE(sat)}$. When the transistor switches to cutoff, output voltage of the circuit rises toward the level

$$V_{out} = \frac{V_{CC}R_T}{R_L + R_T} \tag{8-15}$$

where V_{out} is the maximum positive output-voltage level. Figure 8-2*b* shows an emitter-follower transistor Q_2 connected between the collector of transistor Q_1

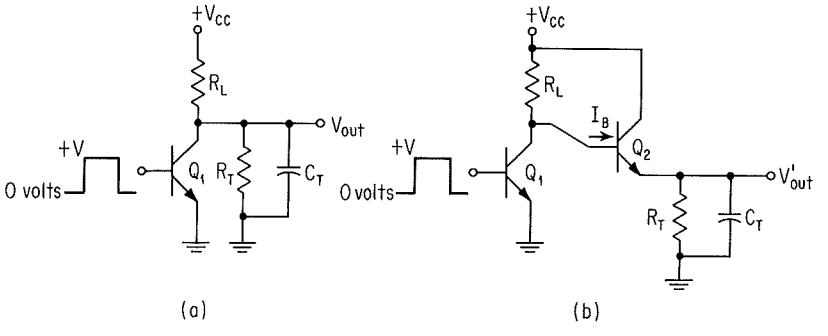


Fig. 8-2. Application of the emitter-follower as an impedance transformer. *(a)* **Load driven by current flow through** R_L; *(b)* **use of emitter-follower to drive load.**

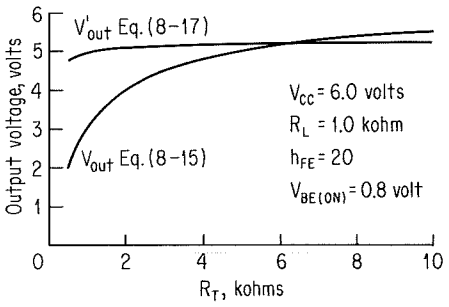


Fig. 8-3. Plots of Eqs. (8-15) and (8-17).

and the external load. For Q_1 at cutoff, voltage across the parallel combination of R_T and C_T can be expressed

$$V'_{\text{out}} = V_{CC} - I_B R_L - V_{BE(\text{ON})} \tag{8-16}$$

where V'_{out} is the maximum positive output-voltage level. Current I_B is related to I_E and consequently to V'_{out}. The I_B term in Eq. (8-16) can be replaced by $V'_{\text{out}}/R_T(h_{FE} + 1)$ to yield

$$V'_{\text{out}} = \frac{V_{CC} - V_{BE(\text{ON})}}{1 + R_L/[R_T(h_{FE} + 1)]} \tag{8-17}$$

Typical plots of Eqs. (8-15) and (8-17) are shown in Fig. 8-3 for various values of R_T. A V_{CC} of 6 volts and an R_L of 1.0 kilohm are assumed. Transistor Q_2 is considered to have an h_{FE} of 20 and a constant $V_{BE(\text{ON})}$ voltage drop of 0.8 volt.* This latter figure shows that for emitter-follower coupling, output voltage is less dependent upon external load resistance. In addition, the emitter-follower stage gives a larger output voltage for low values of R_T.

If the right side of Eq. (8-4) is substituted for I_E in Eq. (8-9) and the resulting expression solved for I_B, there results

$$I_B = \frac{V_{\text{in}} - V_{BE(\text{ON})}}{R_E(h_{FE} + 1)} \tag{8-18}$$

Figure 8-4 shows a circuit for which Eq. (8-18) is valid. External resistance at the emitter terminal is effectively $h_{FE} + 1$ times as large when viewed from the base terminal. Equation (8-14) indicates that, to a reasonable approximation, ac impedance at the emitter terminal is multiplied by $h_{FE} + 1$ in order to be transformed into the base circuit. If the ac load is a capacitor, this load appears at the base terminal as the capacitance value *divided* by $h_{FE} + 1$. An equivalent circuit to represent the emitter-follower stage of Fig. 8-2*b*, with respect to the base terminal, is given in Fig. 8-5. This latter equivalent circuit is exact for dc analysis and is valid for small-signal analysis insofar as $h_{fe} \approx h_{FE}$ and ac impedance of the base-emitter diode can be neglected.

Rise time of the output-voltage waveform is lower in the circuit of Fig. 8-2*b* than in the circuit of Fig. 8-2*a*. With the emitter-follower connection, effective load

* The actual voltage drop decreases slightly for larger values of R_T.

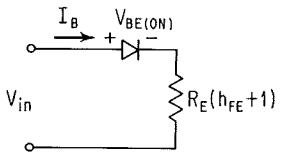


Fig. 8-4. Equivalent circuit for Eq. (8-18).

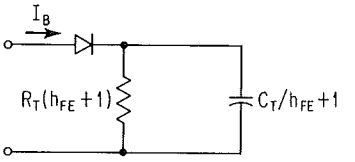


Fig. 8-5. Equivalent circuit for input portion of emitter-follower stage in Fig. 8-2*b*.

capacitance of the inverter stage is reduced by the factor $h_{FE} + 1$, and collector voltage of transistor Q_1 reaches a given level in less time than if the emitter-follower stage were not used. Three measured plots of output voltage level versus time are given in Fig. 8-6, together with the two test-circuit configurations. A comparison of curves V_A and V_B shows that use of an emitter-follower stage to drive load capacitance does decrease fall time of an inverter stage. Curves V_B and V_C show that there is little delay associated with the emitter-follower stage. Base-emitter voltage drop of the emitter-follower transistor prevents V_B from attaining the final amplitude of V_C.

Charge-storage effects do not exist in a well-designed emitter-follower circuit, as the transistor does not saturate. Generally, when an emitter-follower stage is driven by an inverter stage, as shown in Fig. 8-2*b*, the same collector supply voltage is used for the two stages. Since collector voltage of the inverter transistor cannot become more positive than the collector supply voltage, the emitter-follower transistor cannot saturate.

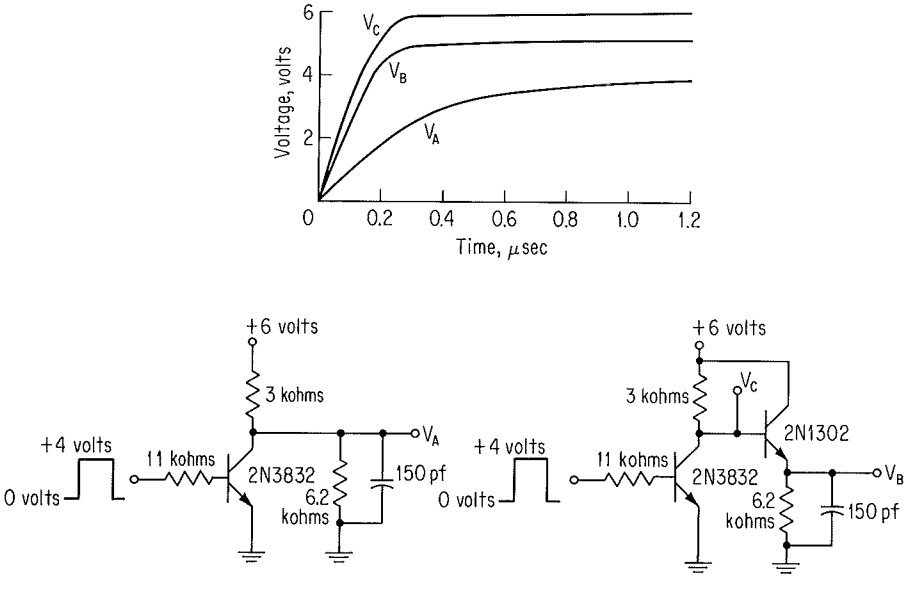


Fig. 8-6. Measured voltage plots for the two test circuits.

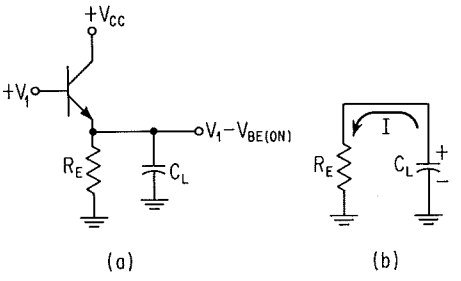


Fig. 8-7. Circuits to show charge and discharge paths for load capacitance. *(a)* **Emitter-follower charges capacitance;** *(b)* **capacitor discharges through R_E.**

Turnoff time of an emitter-follower stage is dependent upon resistance and capacitance of the load. This is illustrated by the circuit diagrams of Fig. 8-7. For a positive input signal V_1 (Fig. 8-7*a*), the load capacitor charges to a value $V_1 - V_{BE(ON)}$. When the input signal falls below the V_1 level, the transistor cuts off, and the capacitor must discharge through the load resistor as shown in Fig. 8-7*b*. The transistor cannot discharge the capacitor, and the output-voltage waveform decays at a rate determined by R_E and C_L. Turnoff time of the output-voltage waveform can be decreased by connecting R_E to a negative voltage, connecting a diode across the base-emitter terminal of the transistor, or by use of a complementary emitter-follower circuit. These three circuit configurations are described in Secs. 8-3 and 8-5.

Power dissipation of an emitter-follower transistor may be considerably larger than that of a saturated inverter. Since the emitter-follower transistor does not saturate, collector-emitter voltage of the device may be as large as several volts, depending upon levels of base-input signal and collector supply voltage.

Oscillations are often observed on the output waveform of an emitter-follower stage. When the emitter-follower transistor drives a capacitive load, input impedance of the device has a negative real part over a range of high frequencies.[1-3] Input impedance is a complex quantity and has a capacitive component over a wide frequency spectrum. If a signal line having an inductive component of impedance is connected to the base of the transistor, a circuit of the type shown in Fig. 8-8 exists at the input to the emitter-follower stage. This circuit will oscillate at the frequency where $X_L = X_C$, provided that $|-R_1| \geqslant |R_2|$.[2]

Careful layout of components, including minimization of wire lengths and stray wiring capacitance, can often eliminate the oscillations described above. Other solutions to the oscillation problem follow:[1,2]

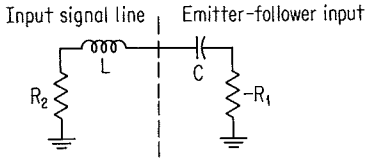


Fig. 8-8. Input-circuit conditions which may cause emitter-follower to oscillate.

1. Use a smaller emitter resistance in parallel with the load capacitance.
2. Increase base resistance.
3. Increase emitter resistance in series with the load capacitance.
4. Add feedback from collector to base of the transistor.
5. Use a ferrite core as a single-turn transformer in the emitter circuit.

The first method of eliminating oscillation increases collector current and consequently power dissipation of the transistor. The remaining four approaches degrade transient response of the circuit.

8-3. EMITTER BIASING

Current flows in a transistor only when voltage across the base-emitter diode exceeds a certain threshold level. For an emitter-follower circuit in which the emitter resistor is connected to ground potential, the input-voltage level required for turn-on is determined largely by whether the transistor is a germanium or a silicon device.* This input-voltage threshold is approximately 0.15 volt for a germanium device and approximately 0.5 volt for a silicon device. Thus, the emitter-follower circuits described above are at cutoff when the input signal is at ground potential.

Emitter-follower circuits are often biased as shown in Fig. 8-9. The emitter-supply voltage is sufficiently negative to forward-bias the base-emitter junction for input signals more positive than $-|V_{EE}| + |V_{BE(ON)}|$. The magnitude of $-V_{EE}$ is chosen such that the transistor does not cut off for even the most negative level of input signal. The transistor now operates in a region of relatively high f_T, and transient response of the circuit is improved.

Emitter-bias voltage reduces discharge time of the capacitive load shown in Fig. 8-10. Consider that $-V_{EE}$ can be varied from zero volts to a large negative level and that resistor R_E can be simultaneously varied to maintain a constant dc value of emitter current I_E. For a constant value of I_E, a curve of decay time versus $-V_{EE}$ can be plotted to show the effect of $-V_{EE}$ upon turnoff time of the circuit. The value of R_E is given by

$$R_E = \frac{V_1 - V_{BE(ON)} + V_{EE}}{I_E} \tag{8-19}$$

For a sudden decrease of input-signal level to zero volts,

$$V_{out} = -V_{EE} + [V_1 - V_{BE(ON)} + V_{EE}]e^{-t/R_E C} \tag{8-20}$$

* Doping levels and geometry of the transistor have a secondary effect upon turn-on voltage of the base-emitter diode.

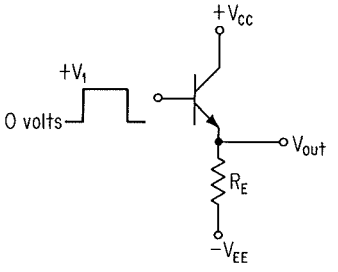


Fig. 8-9. Connection of R_E to a negative supply voltage improves turn-on response of emitter-follower stage.

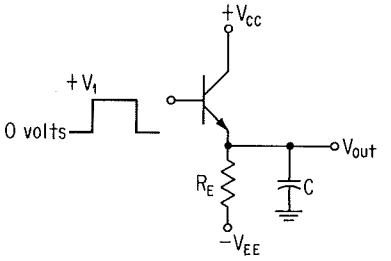


Fig. 8-10. Negative supply voltage reduces turnoff time for a capacitive load.

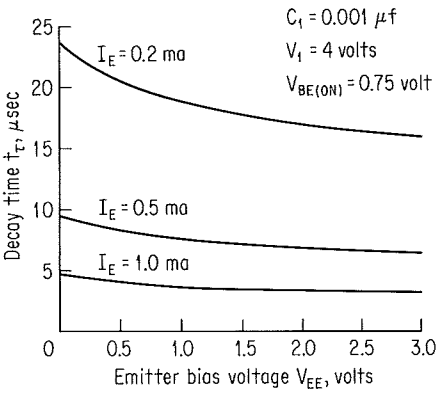


Fig. 8-11. Calculated plots of t_τ versus $-V_{EE}$ for three values of I_E.

where V_{out} cannot decrease below the $-V_{BE(\text{ON})}$ level (because of the zero-level input signal).

Let decay time be defined as the time interval required for the output-voltage waveform to fall from the $V_1 - V_{BE(\text{ON})}$ level to 0.75 volt. The right side of Eq. (8-20) is set equal to 0.75 volt, and decay time is determined to be

$$t_\tau = -R_E C \ln \frac{V_{EE} + 0.75}{V_1 - V_{BE(\text{ON})} + V_{EE}} \tag{8-21}$$

Figure 8-11 shows calculated plots of t_τ versus $-V_{EE}$ for three values of I_E. The following circuit constants are assumed for these plots:

$$C = 0.001 \ \mu\text{f}$$
$$V_1 = 4 \text{ volts}$$
$$V_{BE(\text{ON})} = 0.75 \text{ volt}$$

This latter figure shows that decay time decreases as the emitter-bias voltage is made more negative. Although power dissipation in the transistor does not increase if I_E is maintained constant, total power dissipation of the circuit increases as $-V_{EE}$ is made more negative.

8-4. GRAPHICAL ANALYSIS OF THE EMITTER-FOLLOWER CIRCUIT

The circuit designer is generally concerned with output-voltage level and emitter current of the emitter-follower circuit for any particular value of input signal. Output-voltage level of the conducting emitter-follower transistor is equal to the base-input voltage minus $V_{BE(\text{ON})}$ of the device. Emitter current of the transistor is dependent upon voltage across the emitter resistor and consequently upon $V_{BE(\text{ON})}$ of the device. Because of the nonlinear relationship existing between $V_{BE(\text{ON})}$ and I_E of a transistor, graphical techniques are well suited to analysis of emitter-follower operation.

Graphical circuit analysis is applied below to an emitter-follower circuit of the type shown in Fig. 8-9. Similar considerations apply to the various other types of emitter-follower circuits described in this chapter. Three different types of

base-input circuits are considered; two of the circuits utilize a voltage drive, and the third circuit employs a transistor inverter to drive the emitter-follower base.

Voltage Drive. An emitter-follower circuit driven by input voltage V_{in} is shown in Fig. 8-12*a*. Figure 8-12*b* shows the relevant portion of the circuit under consideration, where the base-emitter junction is represented by a diode. The collector-current generator is omitted from this latter diagram for simplicity. Currents I_1 and I_2 are at the *emitter* side of the base-emitter diode; since the transistor does not saturate, the I_E versus V_{BE} diode characteristic of Fig. 7-13 (for $V_{CE} = 5$ volts) is used in the analysis. Current I_2 is plotted in Fig. 8-12*c*, together with plots of I_1 for two values of V_{in}. The intersection of the I_2 plot with an I_1 plot gives the level of emitter current for a particular value of V_{in}. Base current can be obtained by dividing emitter current by $h_{FE} + 1$.

If an external base resistance is included in the emitter-follower stage, base current of the transistor must be considered in the circuit analysis. Figure 8-13*a* shows an emitter-follower circuit having an external base resistance, and Fig. 8-13*b* is an equivalent-circuit representation of the emitter-follower stage. One method of obtaining the relationship between V_{in} and V_{out} is to determine required values of V_{in} to give various assumed values of V_{out} in Fig. 8-13*b*. This is accomplished as follows. Assume a value for V_{out} which is not more negative than the level

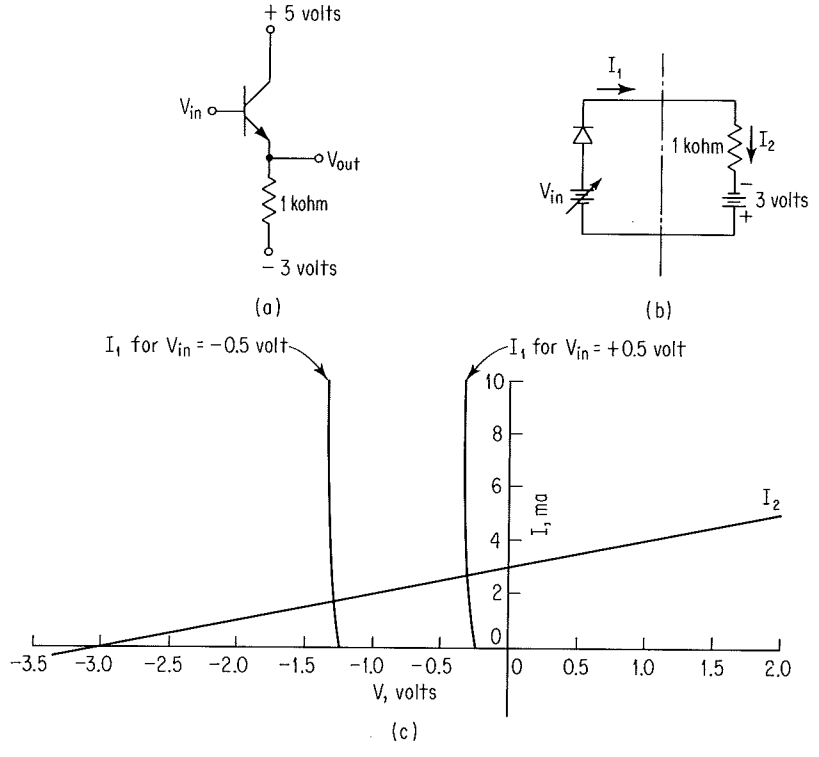


Fig. 8-12. Dc analysis of emitter-follower stage. *(a)* **Emitter-follower circuit;** *(b)* **equivalent circuit;** *(c)* **graphical analysis.**

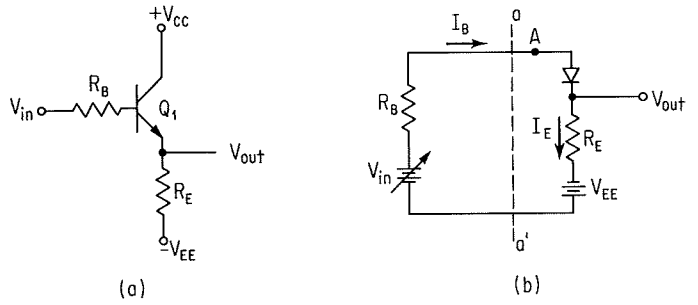


Fig. 8-13. *(a)* **Emitter-follower stage having external base resistor;** *(b)* **equivalent circuit for obtaining relationship between V_{in} and V_{out}.**

of V_{EE}. The difference between V_{EE} and V_{out} is then divided by R_E to obtain I_E. From a plot of I_E versus V_{BE}, voltage drop across the diode can be obtained. This voltage drop is then added to the assumed value of V_{out} to obtain voltage at point A in the above diagram. Current I_B is determined by dividing I_E by $h_{FE} + 1$, where h_{FE} is dc current gain at the particular level of I_E. Now that current through R_B, magnitude of R_B, and voltage at point A are known, the required value of V_{in} can readily be determined.

As an example of the above method of circuit analysis, consider that the emitter-follower stage of Fig. 8-13*a* is implemented in the following manner:

Q_1: 2N3832 transistor having the I_E versus V_{BE} characteristic of Fig. 7-13.
R_E: 1-kilohm resistor.
R_B: 3-kilohm resistor.
$-V_{EE}$: −3-volt dc voltage
V_{CC}: +5-volt dc voltage.

The equivalent circuit of Fig. 8-13*b* is referenced throughout the following discussion. For an assumed V_{out} of 0 volts, I_E is calculated to equal 3 ma. The I_E versus V_{BE} plots of Fig. 7-13 show that for a V_{CE} of 5 volts, an I_E of 3 ma corresponds to a V_{BE} of 0.82 volt. This value of V_{BE} is added to V_{out} to obtain 0.82 volt at point A. The transistor has an h_{FE} of 39.2 at the assumed operating point, and I_B is determined to have a value of 0.0765 ma. This current flow gives a 0.23-volt drop across the 3-kilohm base-input resistor. The 0.23-volt drop is added to voltage at point A to obtain a voltage of 1.05 volts for V_{in}.

For V_{out} levels other than 0 volts, V_{CE} is not equal to 5 volts. However, the plot of I_E versus V_{BE} used above will give reasonably accurate results. The circuit described above was fabricated, and V_{out} was measured for various levels of V_{in}. Figure 8-14 shows plots of measured and calculated values for V_{out} as a function of V_{in}.

A second method of graphically determining V_{out} for various values of V_{in} involves a transformation of the emitter resistance into the base circuit. This transformation is accomplished by multiplying R_E by the term $h_{FE} + 1$, as described previously in Sec. 8-2. Figure 8-15 shows an equivalent circuit for the emitter-follower stage of Fig. 8-13*a*. Only base current flows in the equivalent

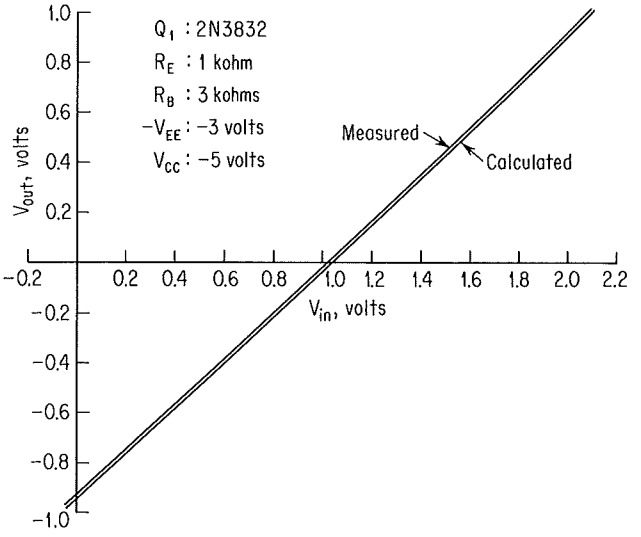


Fig. 8-14. Measured and calculated plots of V_{out} versus V_{in} for circuit of Fig. 8-13*a*.

circuit, and a plot of I_B versus V_{BE} can be used for a graphical analysis of current and voltage levels. Because h_{FE} of the transistor is not constant for all levels of emitter current, this latter method of graphical analysis is not so accurate as the previous method, in which a value of V_{out} is assumed and a value of V_{in} is calculated.

Transistor Drive. The input-voltage level to the emitter-follower transistor in Fig. 8-16*a* is controlled by current flow through the inverter transistor. If the inverter is not allowed to saturate, the emitter-follower stage, together with the output portion of the inverter stage, can be represented by the equivalent circuit of

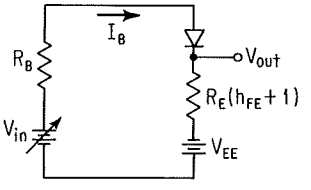


Fig. 8-15. Alternate equivalent circuit for emitter-follower stage of Fig. 8-13*a*.

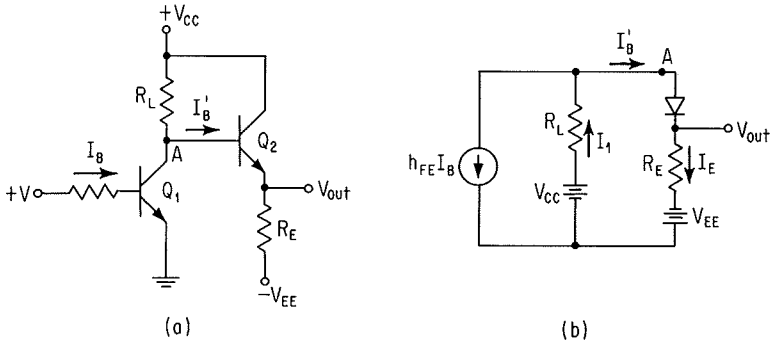


Fig. 8-16. *(a)* Cascade connection of inverter and emitter-follower stages; *(b)* equivalent representation of entire circuit for Q_1 out of saturation.

Fig. 8-16*b*. Collector current of transistor Q_1 is shown as $h_{FE}I_B$. Current I_1 is seen to be the sum of currents $h_{FE}I_B$ and I_B'. Voltage at point A and current I_B' can be determined for an assumed value of V_{out}. The value of I_1 required to sustain the calculated voltage at point A can readily be determined. Current I_B' is then subtracted from I_1 to yield current $h_{FE}I_B$. The input circuit to the inverter stage can then be subjected to an analysis (described in Sec. 6-2) which gives the required value of V_{in} to obtain the desired $h_{FE}I_B$ level.

Suppose that transistor Q_1 in Fig. 8-16*a* is allowed to saturate. The equivalent circuit shown in Fig. 8-17*a* yields reasonably accurate values of V_{out} for various levels of V_{in} to the inverter stage. The value of $r_{CE(sat)}$ in the equivalent circuit is the collector-emitter saturation resistance for the particular level of base current to Q_1.* A composite *VI* plot is shown in Fig. 8-17*b* for the portion of the equivalent circuit to the right of line *aa'*. The *VI* plot for the circuit branch containing $r_{CE(sat)}$ is also shown in this latter diagram. The intersection of the two plots gives voltage across each of the three branches of the equivalent circuit; this voltage

* Resistance $r_{CE(sat)}$ is obtained by dividing $V_{CE(sat)}$ by the I_C level at which the saturation voltage is measured.

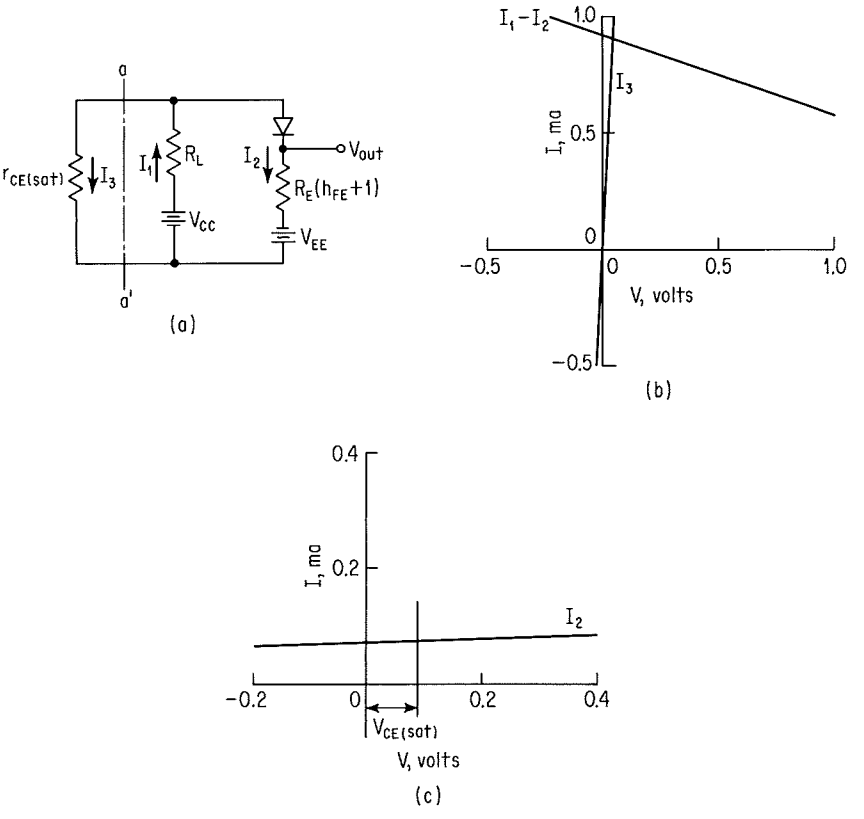


Fig. 8-17. *(a)* **Equivalent representation of circuit in Fig. 8-16*a* for Q_1 in saturation;** *(b)* **graphical determination of $V_{CE(sat)}$;** *(c)* **graphical determination of V_{out}.**

is $V_{CE(sat)}$ of Q_1 for the above loading. The two plots shown in Fig. 8-17*c* are used to determine V_{out} of the circuit. A *VI* curve for that branch of the equivalent circuit containing the diode, resistor R_E, and voltage V_{EE} is plotted, together with a vertical line located at the $V_{CE(sat)}$ level. The intersection of these two plots gives the current level in the above branch. Voltage drop across $R_E(h_{FE} + 1)$ can now be calculated, and V_{out} can be determined.

8-5. DESIGNS FOR SINKING LOAD CURRENT

Although the N-P-N emitter-follower stage serves well as a source of current into an external load, the circuit configurations described to this point are not suitable for sinking an appreciable load current. When the transistor in the simple emitter-follower circuit of Fig. 8-1 is at cutoff, the emitter resistor can sink only a limited amount of current from an external current source. This current flow through the emitter resistor causes voltage drop across the resistor, and output voltage of the circuit is generally much higher than if a saturated N-P-N inverter stage were used to sink the load current. The discussion of Sec. 8-3 pointed out that discharge time of a load capacitance is reduced if the emitter resistor is returned to a negative emitter-bias voltage. The negative-voltage return also enables emitter-terminal voltage to drop to a lower level than that attained by the circuit of Fig. 8-1; consequently, the emitter resistor can sink a larger current if it is connected to a negative supply voltage, although at the expense of increased power dissipation.

One method of improving the current-sinking capability of an emitter-follower stage is to add a diode to the emitter-follower transistor, as shown in Fig. 8-18. For positive-level input signals, the diode is reverse-biased and is unable to conduct current, When the input signal falls to a low potential, the diode conducts, and load current I_L flows through the low-impedance path consisting of the diode and signal source. In addition, the diode serves as a voltage clamp to prevent the output voltage from rising significantly above the input-voltage level. Rise time of the output-voltage waveform is deteriorated slightly by depletion-layer capacitance of the reverse-biased diode.

A disadvantage of the above circuit connection is that current from the external load flows into the signal source connected to the emitter-follower base. If this signal source is a transistor inverter, the transistor must be capable of conducting the additional load current. An emitter-follower stage is shown in Fig. 8-19 which can sink a reasonably large load current and yet not allow a significant amount of current to flow into the inverter stage. The base-emitter diode of the P-N-P transistor has a forward conduction path for load current which is into the emitter terminal of the device. Because of transistor action, base-current flow out of the P-N-P

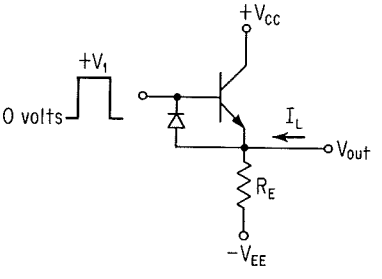


Fig. 8-18. Diode connected across base-emitter junction allows external-load current to flow into signal source.

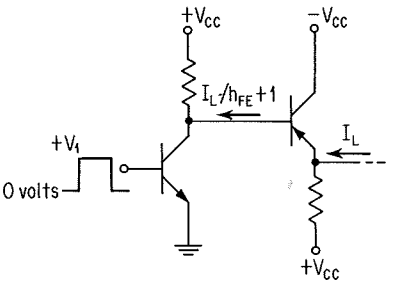


Fig. 8-19. Use of P-N-P emitter-follower permits relatively large load current to be sinked.

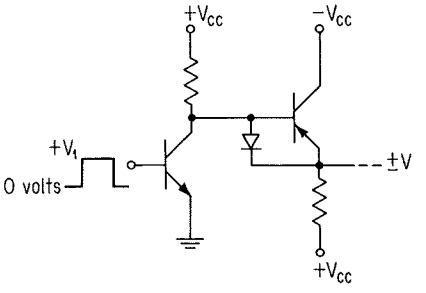


Fig. 8-20. External-load current is sourced through diode and is sinked by emitter of P-N-P.

device is equal to $I_L/(h_{FE} + 1)$. The emitter-follower stage is now unable to source a large current to the external load. Addition of a diode across the base-emitter terminal of the P-N-P transistor, as shown in Fig. 8-20, improves the current-driving capability of the P-N-P emitter-follower stage. However, this latter circuit is inferior to the N-P-N emitter-follower circuit as a current *source.*

For either polarity of input-voltage pulse, the positive- and negative-going edges of the pulse are preserved at the output terminal by the N-P-N and P-N-P emitter-follower transistors, respectively. Addition of a diode across the base-emitter junction of either of the two transistor types enables the circuit better to conduct the opposite-polarity current to that of the forward-biased base-emitter diode. Although the added diode gives an overall improvement in circuit performance, one edge of the output-voltage waveform is generally less well preserved than the other edge.

A complementary emitter-follower circuit can be connected as shown in Fig. 8-21 to drive the output load in both the positive- and negative-going directions. The N-P-N transistor provides a low-impedance drive for current into the load, and the P-N-P transistor is a low-impedance sink for current from the load. Since base current of either transistor is considerably less than emitter current of the device, there is little loading of the input-signal source.

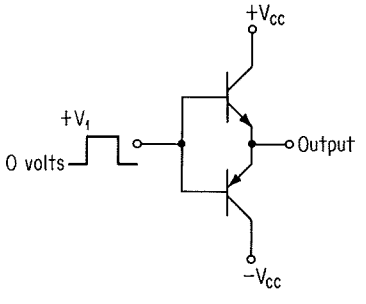


Fig. 8-21. Complementary emitter-follower gives positive driving action for leading and trailing edges of output signal.

It is important that the two transistors in a complementary emitter-follower circuit turn on and off in approximately equal times. If one transistor turns on before the other turns off, a low-impedance path will exist between collector terminals of the two devices. In order to prevent excessive collector-current flow during the above circuit condition, series limiting resistors are often connected in each collector lead. The presence of a collector resistor causes a voltage swing at the collector terminal; this results in a larger voltage differential across the collector-base junction and

additional time is required to charge C_{ob}. Another consideration which limits size of the collector resistor is that the transistor may saturate if the resistor becomes large. External series resistance at each collector lead of the complementary emitter-follower is generally restricted to values less than 50 ohms.

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9

Symbolic Logic

9-1. INTRODUCTION

Individual electronic switching networks can be organized into larger functional blocks which will provide known output-signal levels for various combinations of input-signal levels. Mathematical expressions can be written to describe the electrical state of one or more of the above switches; these expressions can be combined in accordance with certain rules, and the electrical state of each output-signal line can be described for any combination of input-signal lines.

Symbolic logic, utilized for the above mathematics, uses only the numerals 0 and 1. These two digits constitute a numbering system known as the "binary number system." This chapter describes the binary number system and presents the necessary background for an understanding of the application of symbolic logic to switching networks.

9-2. BINARY NUMBER SYSTEM

The binary number system can best be described by analogy to the decimal number system. The decimal number system utilizes the arabic numerals 0 to 9 in a shorthand notation for certain arithmetic operations. Each digit in a decimal number is actually multiplied by a power of 10; the various products are then summed together to yield the decimal quantity. The power of 10 by which a digit is multiplied is determined by the position of the digit within a given sequence. For instance, the sequence of numerals 1,352 is interpreted as $1 \times 10^3 + 3 \times 10^2 + 5 \times 10^1 + 2 \times 10^0$; the various products can be formed to yield $1{,}000 + 300 + 50 + 2$. Summation of the last group of digits yields the quantity one thousand three hundred fifty-two. Because the decimal number system is so familiar, the above arithmetic steps are generally omitted, and a given sequence of numerals is immediately interpreted as a particular quantity. In the binary number system, the arabic numerals 0 and 1 are the only digits used. By combining these binary digits, or bits, in the proper manner, decimal numbers can be represented. For the present analysis, only integer decimal values will be considered. In order to represent a decimal number, the bits 0 and 1 are written in a sequence. The various bits in a binary sequence are multiplied by powers of 2,

and the position of a bit determines the power of 2 by which the bit is to be multiplied. The sequence is often written from right to left, with the most significant bit to the extreme left. This convention will be followed in the present discussion. Let the bit position at the extreme right in the sequence represent $2^0 = 1$; then the second bit position from the right represents $2^1 = 2$. Each additional position to the left represents an additional power of 2. The binary number

$$1011$$

is interpreted, from left to right, as

$$1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$$

which is equal to the decimal number 11. Table 9-1 shows the decimal numbers 0 through 15 written in binary notation.

Larger decimal numbers than those shown in the above table can be written in binary form by increasing the number of bit positions. For a given number of bits in a binary sequence, the *total* number of distinct decimal magnitudes which can be written in the binary code is given by

$$\text{Total number of decimal magnitudes} = 2^n$$

where n is the number of bit positions. There are four bit positions in Table 9-1, and a total of $2^4 = 16$ separate decimal numbers can be written with the four-bit binary sequence. The table shows the 16 decimal numbers (0 through 15) which the four bits can represent.

Noninteger decimal numbers can be represented by assigning negative powers of 2 to certain of the bit positions. If a 1 appears in the 2^{-1} bit position, the decimal number 0.5 is indicated. Additional negative powers of 2 allow smaller fractional decimal values to be written.

Table 9-1. Binary Notation for Decimal Numbers 0 to 15

Decimal number	2^3	2^2	2^1	2^0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

9-3. BINARY NATURE OF SWITCHES

A switching circuit generally has the two stable states of ON or OFF. One of these states can be regarded as a binary 0, with the second state considered as a binary 1. In this manner, the bits 0 and 1 can be used to represent the two states of a bistable switch. Conversely, the state of a bistable switch can be used to represent either of the two binary digits. As an example of the above application of switches, consider the circuit of Fig. 9-1. In the present discussion, the positive output-voltage level of a nonconducting transistor and the relatively negative ($V_{CE(sat)}$) output-voltage level of a saturated transistor are defined to represent the bits 1 and 0 respectively. For the bias conditions shown in the figure, transistor Q_1 is at cutoff, while transistors Q_2 and Q_3 are in saturation. Output voltage levels of the circuit are seen to represent the binary number 100.

Eight different decimal numbers can be represented by the circuit of Fig. 9-1. If the same information were to be stored in decimal notation, a circuit having eight distinct states would be required. This could be accomplished, for instance, by utilizing eight separate bistable switches, where any one of the switches can be in a different state from all others. The eight separate switches can then be used to store any one of eight numbers.

Because of the ease with which switches can be used to represent binary digits, and also because the bits 0 and 1 can be used to denote the state of a switch, the binary number system is widely used in conjunction with transistor switching circuits. Various modifications of the binary number system are often employed in the arithmetic portions of electronic digital computers.[1,2] However, as the binary notation described in Sec. 9-2 is well suited to a mathematical analysis of the state of a transistor switch, this binary notation, and also the modified version described below, are the only two forms of binary notation to be considered. The one variation in the above binary system is the order of ascending powers of 2. It will later be convenient to write binary numbers from left to right, instead of from right to left as described earlier.

When binary symbols are used to indicate the state of a transistor switch, there is not necessarily the intention of representing a digital number. The binary outputs of transistor switches are generally interpreted for their decimal equivalents only in counter and storage elements.

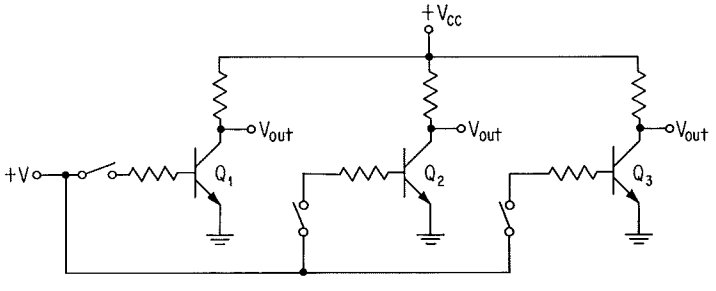

Fig. 9-1. Use of transistor inverters to represent binary digits 0 and 1.

9-4. MATHEMATICS OF LOGIC

In order to evaluate logical propositions in a straightforward manner, a mathematics of logic was developed. This mathematics is generally known as "Boolean algebra," in honor of George Boole, who in 1854 wrote a description of this logical language.[3] Simply stated, the algebra is based upon the principle that a proposition of logic is either true or false. The true propositions are given the number 1 and the false propositions are assigned the number 0.

Two mathematical operations OR and AND are employed in Boolean expressions. In general, the OR function is denoted by + and the AND function is denoted by $\times$, a dot, parentheses, or simply no notation between two adjacent symbols.[4,5] The nomenclature used here is the + sign for OR and an indicated multiplication for AND. The expression $A + B$ is read "A OR B" and the expression AB is read "A AND B." An expression such as $(A + B)\ (C + D)$ is read "A OR B AND C OR D."

Six postulates, or rules, of Boolean algebra are given below. These postulates can be used to evaluate various logical expressions.

$$0 + 0 = 0 \tag{9-1}$$

$$0 + 1 = 1 \tag{9-2}$$

$$1 + 1 = 1 \tag{9-3}$$

$$0 \cdot 0 = 0 \tag{9-4}$$

$$0 \cdot 1 = 0 \tag{9-5}$$

$$1 \cdot 1 = 1 \tag{9-6}$$

With respect to the postulates that include the OR operation, it is seen that the result is 1 if at least one of the terms on the left side of the expression is 1. The AND operation yields 1 only when both terms on the left are 1.

Letters are often used in the equations of Boolean algebra to represent variable quantities. Each of these letters may take on a value of 1 or of 0. The expression

$$A + B = C \tag{9-7}$$

indicates that the value of C is determined by an OR operation upon values of A and B. There are four possible combinations of 0 and 1 which can be substituted into the above expression. For each combination of the variables A and B, postulates (9-1) to (9-3) can be used to obtain the value of C. A listing of the various values of A and B, together with each resulting value of C, is referred to as a "truth table." A truth table for Eq. (9-7) is given in Table 9-2.

Table 9-2. Truth Table for $A + B = C$

A	B	C
0	0	0
1	0	1
0	1	1
1	1	1

Table 9-3. Truth Table for $AB = C$

A	B	C
0	0	0
1	0	0
0	1	0
1	1	1

If the letters A and B are combined in the AND function, the expression is written

$$AB = C \tag{9-8}$$

Table 9-3 is a truth table for the above AND operation.

Logical expressions may contain more terms than those shown in Eqs. (9-7) and (9-8). As in ordinary algebra, equivalent expressions may be obtained by factoring, combining, or expanding terms. The associative, commutative, and distributive laws of ordinary algebra apply to the OR and AND operations.[6] From the associative laws for addition and multiplication,

$$A + (B + C) = (A + B) + C \tag{9-9}$$

$$A(BC) = (AB)C \tag{9-10}$$

The commutative laws for addition and multiplication give

$$A + B = B + A \tag{9-11}$$

$$AB = BA \tag{9-12}$$

The distributive law yields

$$A(B + C) = AB + AC \tag{9-13}$$

The above expressions are actually Boolean identities. Equations (9-9) to (9-12) are obviously valid in Boolean algebra. However, because Boolean algebra is *not* identical to ordinary algebra, there may be some question as to the validity of Eq. (9-13). The *truth* of this latter expression can be verified by application of a truth table. Table 9-4 shows the eight possible combinations of variables A, B,

Table 9-4. Truth Table for $A(B + C) = AB + AC$

(1) A	(2) B	(3) C	(4) $C + B$	(5) $A(C + B)$	(6) AB	(7) AC	(8) $AB + AC$
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0
1	1	0	1	1	1	0	1
0	0	1	1	0	0	0	0
1	0	1	1	1	0	1	1
0	1	1	1	0	0	0	0
1	1	1	1	1	1	1	1

and C, together with the results obtained from various groupings of the three variables. Column 4 gives the result for $C + B$: the result is equal to 1 when either C OR B is equal to 1. The values in column 4 are then *ANDed* together with variable A and listed in column 5. This latter column is an evaluation of the left side of Eq. (9-13) for the eight possible combinations of A, B, and C. Columns 6 and 7, respectively, of the table show values of AB and AC for the various combinations of A, B, and C. The results of columns 5 and 6 are then *ORed* together in column 8. A comparison of columns 5 and 8 shows that Eq. (9-13) is indeed valid.

The above method of verifying a Boolean identity is one of "perfect induction."[6] All possible combinations of variables are substituted into an expression, and the resulting truth table is compiled. The truth table shows whether or not the expression is correct.

Several differences exist between ordinary algebra and Boolean algebra. A Boolean expression containing a variable and the number 1 or 0 represents a logical operation and must be evaluated in accordance with postulates (9-1) to (9-6). For instance, postulates (9-2) and (9-3) show that

$$A + 1 = 1 \tag{9-14}$$

and postulates (9-5) and (9-6) show that

$$A \cdot 1 = A \tag{9-15}$$

The six postulates can also be used to obtain

$$A + A = A \tag{9-16}$$

and

$$A \cdot A = A \tag{9-17}$$

In ordinary algebra, the expression $AB + B$ can be reduced to $B(A + 1)$. The above reduction is also valid in Boolean algebra, although a further simplification can be made. Equation (9-14) shows that $A + 1$ is equal to 1; this reduces the expression to $B \cdot 1$ which, from Eq. (9-15), yields B alone. The above steps give the Boolean identity

$$AB + B = B \tag{9-18}$$

This identity is valid in ordinary algebra *only* when A is equal to 0.

Since a binary number must be either 0 or 1, the two numbers are said to be *complements* of each other. A letter used to represent a binary number also has a complement. If the letter represents 1, the complement to this letter is 0. Likewise, the complement of the letter takes on the value 1 when the letter itself represents 0. The complement of a letter is the "inverse" of the letter and is usually denoted by the same letter primed or with a bar over the letter; the bar notation will be used throughout this book. The letter A has as its complement the letter $\bar{A}$; this latter symbol is read "not A." One interpretation of the symbols A and $\bar{A}$ is that the former represents the *true* state of the variable and the latter represents the *false,* or *complementary,* state of the variable.

Complementary variables are widely used in Boolean expressions. Two useful

relationships between the true and complementary states of a variable are given below:

$$A + \bar{A} = 1 \tag{9-19}$$

$$A \cdot \bar{A} = 0 \tag{9-20}$$

Postulates (9-2) and (9-5) can be used to verify Eqs. (9-19) and (9-20), respectively. An OR function can be rewritten in the form of an AND function by use of complements. Likewise, complementary notation allows an AND function to be modified to the form of an OR function. The identities

$$ABC \cdots = \overline{\bar{A} + \bar{B} + \bar{C} \cdots} \tag{9-21}$$

$$A + B + C \cdots = \overline{\bar{A}\bar{B}\bar{C} \cdots} \tag{9-22}$$

can be verified by use of truth tables. Equation (9-21) shows that conversion from AND to OR requires taking the inverse of each variable, combining these inverse variables in the OR statement, and taking the inverse of the entire OR function. The transformation from OR to AND in Eq. (9-22) is accomplished by taking the inverse of each variable, combining these inverse variables in the AND statement, and taking the inverse of the resulting AND function.

Many different Boolean expressions may yield the same result. Complex expressions can often be simplified by methods described in the literature.[7,8] However, there is no method of reduction which assures that certain of the more complex functions can be reduced to the minimum number of variables.

9-5. BOOLEAN ALGEBRA APPLIED TO SWITCHING CIRCUITS

In 1938, Shannon wrote a classic paper on the application of Boolean algebra to the design of relay switching networks.[6] Open and closed states of relay contacts were described in terms of 1 and 0, respectively. The mathematics of logic was shown to provide a straightforward method of designing networks composed of switching elements having two stable states. Simply stated, network design consisted of writing a mathematical expression to describe a circuit arrangement of relay contacts; the expression could then be subjected to certain rules of simplification in order to reduce the total number of relay contacts.

The above application of Boolean algebra had a profound effect upon future designs of switching networks. This algebra has since been used extensively to analyze and synthesize circuits which contain elements having two stable states; these elements may be relays, vacuum tubes, transistors, bistable magnetic devices, or other bistable electrical devices. The above circuits perform operations which are described by the algebra of logic and are often referred to as "logic circuits."

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10

Transistors and Diodes as Logic Elements

10-1. BINARY NATURE OF A TRANSISTOR SWITCH

It was pointed out in Sec. 9-3 that the binary digits 0 and 1 can be associated with the cutoff and saturated states of a transistor switch. Either of the two stable states of a transistor switch can be designated as binary 1, with the other stable state representing a binary 0. *Positive logic* interprets the *most positive* signal-voltage level as a binary 1 and the *most negative* signal-voltage level as a binary 0. A second type of logic, *negative logic,* considers that a binary 1 is represented by the *most negative* signal-voltage level; this form of logic assigns binary 0 to the *most positive* signal-voltage level.

Any two stable operating states of a transistor switch can represent the two binary digits. Nonsaturating transistors, and also units which operate well away from either saturation or cutoff, may have two stable operating states. It is necessary that there be a *detectable difference* in voltage or current levels between the two stable states of a transistor switch in order for the correct binary interpretation to be made; the difference in magnitude between the two stable states must be detectable by other circuits of a similar type. The ability of these other circuits to distinguish between the two binary states is increased when the two stable levels have the greatest separation. Transistors which operate from saturation to cutoff have greater voltage variations than those transistors which are not allowed to turn fully on or off. Transistor logic circuits described in this chapter have the two distinct stable states of saturation and collector-current cutoff. Transistor switching circuits of the nonsaturating type are described in Chap. 11.

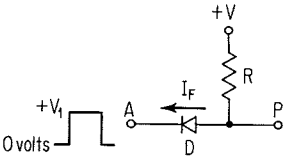


Fig. 10-1. Single-input diode gate.

10-2. DIODE GATES

Figure 10-1 shows a series connection of a diode D, a resistor R, and a positive supply voltage $+V$. This supply voltage is at least a few volts more positive than the most positive input signal to the circuit. Forward diode current I_F flows in the direction shown. An input signal having the two voltage levels of 0 and $+V_1$

volts is applied to the circuit at terminal A. Output voltage of the circuit appears at terminal P and is given by

$$V_P = V_A + V_F \tag{10-1}$$

where V_P = voltage at terminal P
V_A = applied voltage at terminal A
V_F = diode forward-voltage drop

The output-voltage level is seen to be one diode drop larger than the magnitude of diode input voltage. A graphical analysis can be used to determine exact values of V_P for the two extremes of input-voltage level. Output-voltage level of the circuit is controlled by the signal level at terminal A. Because of this gating action upon the output signal, the above circuit is often referred to as a "diode-gate" circuit.[1]

Additional diodes can be added to the basic diode circuit described above; this gives a circuit of the type shown in Fig. 10-2. Input signals which vary from 0 volts (ground potential) to $+V_1$ volts are applied to input terminals A, B, and C of the circuit. If an input terminal, say terminal A, is held at ground potential and input terminals B and C are each connected to $+V_1$ volts, output voltage at terminal P is clamped, by diode D_1, to one diode drop above ground potential. Diodes D_2 and D_3 are reverse-biased, and leakage current I_L flows in each of these devices. Figure 10-3 shows the diode circuit of Fig. 10-2 with the above signal levels.

The above analysis can be extended to include various combinations of signal levels to the three input terminals of the circuit in Fig. 10-2. For any combination of input signals, it would be seen that output-voltage level of the diode circuit is always one diode drop above the *most negative* input voltage. If each input signal is restricted to either the 0- or $+V_1$-volt levels, the output-signal voltage can be *relatively* positive only when all three input-signal levels are at $+V_1$ volts. Thus, voltage at terminal P is relatively positive only when terminal A *and* terminal B *and* terminal C have positive input-voltage levels. If a relatively positive voltage level is regarded as binary 1 (positive logic), a logical expression for the diode circuit can be written

$$P = ABC \tag{10-2}$$

where P, A, B, and C are positive-logic binary levels at the respective terminals. The multiple-input diode circuit of Fig. 10-2 performs the *AND* operation in a *positive-logic* system. On the other hand, voltage at terminal P is relatively *negative* when terminal A *or* terminal B *or* terminal C has a ground-potential input signal. For logic systems in which a relatively negative-voltage level represents binary 1 (negative logic), a logical expression for the diode circuit can be written

$$P = A + B + C \tag{10-3}$$

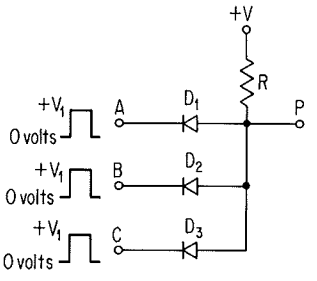


Fig. 10-2. Multiple-input diode gate.

where P, A, B, and C are negative-logic binary levels at the respective terminals. The diode circuit of Fig. 10-2 gives the *OR* function in a *negative-logic* system.

The AND and OR functions of logic circuits are interchanged in positive and negative systems of logic. This was illustrated above for the diode circuit of Fig. 10-2, which performs the AND function for positive logic and the OR function for negative logic. All other logic circuits to be described in this chapter have the dual nature of performing either the AND or OR operations, depending upon which of the two logic systems is used. For this reason, a circuit will be given two logical names, with the *first* name applicable to a *positive* logic system and the *second* name applicable to a *negative* logic system. Thus, the circuit of Fig. 10-2 is classified as an AND/OR circuit.

Diodes in the circuit of Fig. 10-2 may be either germanium or silicon devices. Germanium and silicon diodes have nominal forward-voltage drops V_F of approximately 0.25 and 0.70 volt, respectively. These voltage levels are generally reasonably constant (within 0.1 volt) over a forward current I_F range of roughly 0.1 to 10 ma. Output-voltage level of the circuit is equal to the most negative input-voltage level *plus* V_F. As the magnitude of I_F has only a secondary effect upon V_F, the actual values of circuit output voltage are determined primarily by whether the diode circuit is implemented with germanium or silicon diodes. Silicon diodes, because of their larger forward drop, cause a greater shift between input- and output-signal levels than germanium diodes do. In most logic circuit designs, the exact value of circuit output voltage is not of significance, provided that the "up" levels are above a given threshold value and the "down" levels are below a given threshold value. Because signal voltage levels are generally considerably above or below the threshold values, it usually makes little difference whether silicon or germanium diodes are used in a diode gate.

Design of a logic circuit involves both dc and ac considerations. The dc design assures that the proper voltage levels are present at input and output terminals of the circuit. A suitable ac design enables the circuit to have an adequate transient response. The final choice of circuit parameters is often a compromise between values most suited for ac operation and different values which give optimum dc performance. Pertinent dc and ac design considerations are presented below for the AND/OR diode circuit.

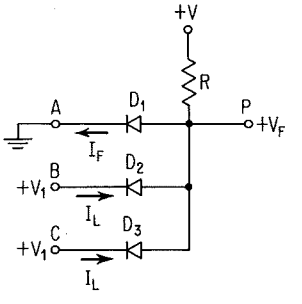


Fig. 10-3. Output voltage of gate clamped to one diode drop above the most negative input signal.

It has been shown how output voltage of the above AND/OR gate is clamped to one diode drop above the lowest input-signal level. If an external-load current flows from the output terminal of the gate, the current causes a voltage drop across R. This voltage drop could conceivably be so large as to reduce output voltage below the level determined by diode clamping. In general, the circuit parameters are selected so that output voltage remains at the clamped level.

Capacitive effects limit operating speed of a diode gate. Figure 10-4*a* shows the diode gate of Fig. 10-2, together with diode capacitance C_D and circuit wiring

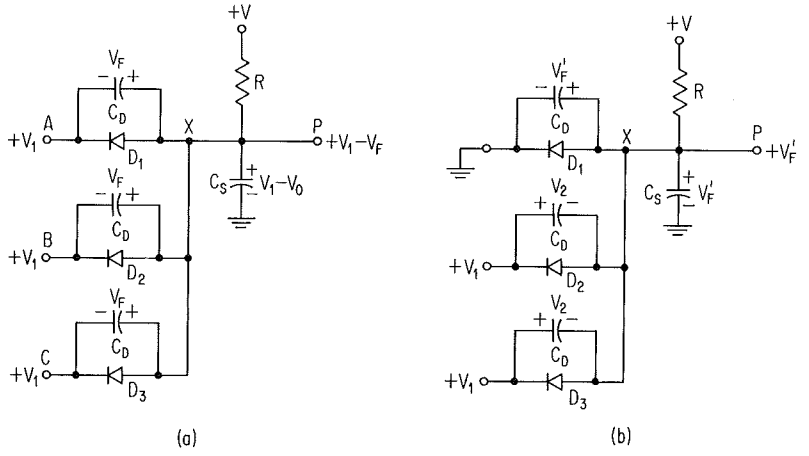


Fig. 10-4. Voltage distribution in diode gate. *(a)* **All input signals positive;** *(b)* **one input signal at ground potential.**

capacitance C_S. For all input terminals at $+V_1$ volts, output voltage of the circuit is at $V_1 + V_F$ volts, and each diode capacitance is charged to V_F volts; this voltage is determined by the diode type, i.e., silicon or germanium, and, to a lesser extent, by the magnitude of current flowing through the diode. Consider that input voltage at terminal A decreases from $+V_1$ to 0 volts. Figure 10-4*b* shows the steady-state circuit conditions which are established some time after terminal A is connected to ground potential. The grounded cathode of diode D_1 causes increased forward current flow in this diode, and voltage drop V_F' is slightly larger than V_F. Output voltage of the circuit has decreased to the V_F' level, and voltage drops across diodes D_2 and D_3 have reversed polarity. Capacitance C_S, as well as the C_D capacitance of each diode, experiences a redistribution of charge before the above steady-state voltage levels are established. Charge flows from C_S and the C_D capacitances of diodes D_2 and D_3 into point X. From point X, the charge flow is divided between D_1 and its associated capacitance. The majority of this charge flows through D_1, as there is only a small voltage change across this diode. Transient response of the decreasing output-voltage waveform is affected by the above charge redistribution. However, as D_1 presents a relatively low impedance path to ground when terminal A is grounded, the negative-going edge of the output-voltage waveform is generally deteriorated only slightly by capacitive effects.

Capacitance of the above circuit has a pronounced effect upon the positive-going edge of the output-voltage waveform. If voltage at input terminal A is instantaneously increased from ground potential to $+V_1$ volts, the various capacitances must charge to the polarities and levels shown in Fig. 10-4*a*. Except for a slight charge contribution from the C_D capacitance across D_1, all charge must now be supplied through resistor R from supply voltage $+V$. The various capacitances experience approximately equal voltage swings, are charged primarily by the $+V$ source, and are discharged largely by the input-signal source. Hence,

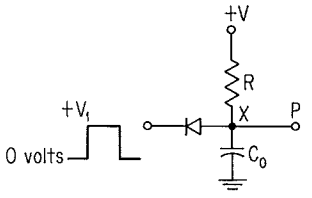


Fig. 10-5. Equivalent circuit of AND/OR diode gate.

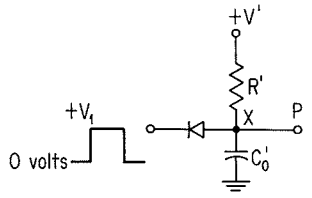


Fig. 10-6. Equivalent circuit of AND/OR diode gate with an external load.

the capacitances are in parallel with each other and can be represented by a single equivalent capacitance C_0 from node X to ground. Output voltage of the gate rises to the steady-state level at a rate determined by $+V$, R, and C_0.

Figure 10-5 shows an equivalent circuit of the above diode gate; this circuit is useful for both a dc and an ac analysis. The one diode shown has an input-voltage level which varies from 0 to $+V_1$ volts. Total circuit capacitance is represented by capacitance C_0. Diode leakage currents are neglected, as they are not significant in the present discussion.*

If an external load is connected to the AND/OR gate, the equivalent circuit can be drawn as shown in Fig. 10-6. Capacitance C_0' represents the parallel combination of diode capacitances, wiring capacitance, and external-load capacitance. Voltage V' and resistance R' are the Thévenin values at point X with the diode disconnected. Output voltage of the gate can rise no higher than the V' level. For an input step of voltage to the $+V_1$ level, voltage at terminal A charges *toward* the V' value at a rate determined by R' and C_0'. The output terminal will be clamped to $V_1 + V_F$ volts *only* if this voltage level is *less positive* than V'; otherwise, output voltage will be at the V' level.

Diode recovery time is often an important consideration in high-speed diode gates. Consider the circuit of Fig. 10-7, in which the diode input signal varies from 0 to $+V_1$ volts. For a ground-potential input signal, the diode is forward-biased, and injected carriers on both sides of the junction migrate by diffusion, drift, or a combination of both effects to the opposite-polarity diode terminals. Upon application of the $+V_1$ signal level, the diode current reverses polarity, and voltage drop across the diode initially decreases only slightly from the forward-voltage drop;[2,3] these two effects are shown in Fig. 10-8, where at time T_0 the input signal is instantaneously increased from 0 to $+V_1$ volts.[4] Two time intervals are shown for the reverse transient response of the diode current and voltage waveforms. The first of these time intervals is given as t_r and is the result of charge storage within the diode. Minority carriers which were previously injected across both sides of the junction are now removed, partly by recombination within the

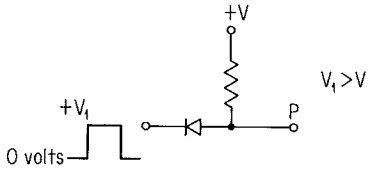


Fig. 10-7. Circuit in which diode can be forward-biased or reverse-biased by input signal.

* The effects of diode leakage current are important in the above circuit when one signal source drives several diodes. This subject is considered in Sec. 10-4.

diode and partly by flowing back to the P or N region from which they were injected; this results in a diode reverse current which remains at a constant level I_R until the injected minority carriers are depleted. The second time interval t_d is the result of charging current into the depletion layer across the reverse-biased junction. Diode voltage decreases to the reverse-bias V_R level at the end of the t_d interval.

Recovery time of the diode, referred to as t_{rr}, is generally defined as the time interval from T_0 to the point on the diode-current waveform where magnitude of the reverse-current transient has decreased from I_R to some arbitrary level; this time is equal to the sum of t_r and a portion of t_d. Figure 10-9 shows transient response of a diode which is switched from I_F to three different values of reverse current. For larger values of reverse current, charge-storage time decreases, thus causing a decrease in reverse recovery time of the diode.

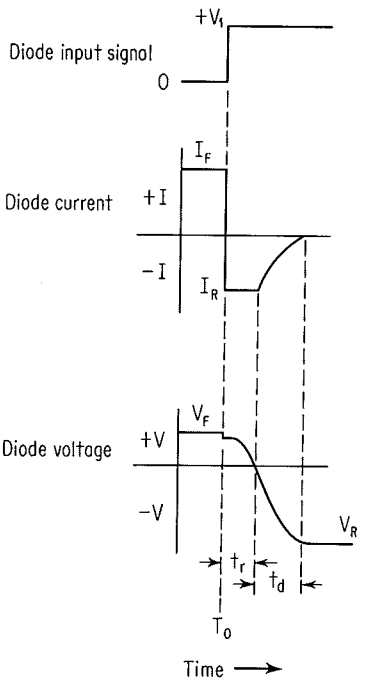


Fig. 10-8. Voltage and current levels in the diode circuit of Fig. 10-7.

Returning now to the AND/OR circuit of Fig. 10-2, let us consider the output-signal level for various combinations of input-signal level. For inputs A, B, and C at ground potential, current from resistor R divides among the three diodes; there is a relatively small voltage drop across any diode, and output voltage of the circuit is close to ground potential. If one of the diode input terminals, say terminal A, is now raised to the $+V_1$ voltage level, the current which was previously flowing through diode D_1 now divides between diodes D_2 and D_3. In addition, a reverse transient current of D_1 flows through D_2 and D_3; this transient current lasts for the recovery duration of D_1. The above two components of current flow cause an increase in output voltage of the circuit. The increase in output-voltage level is even more pronounced if two diode inputs are switched to $+V_1$ volts, with the remaining diode input held at ground potential. Figure 10-10 shows typical input- and output-voltage waveforms for the diode circuit of Fig. 10-2. Inputs A and B are switched to the $+V_1$ level at time T_0; input C remains at ground potential. The output-voltage level is seen to increase from V_F to V_0 volts at T_0 and to remain at this level for the recovery interval of D_1 and D_2. The final value of output voltage is at the V_F level and is determined by dc current flow through D_3.

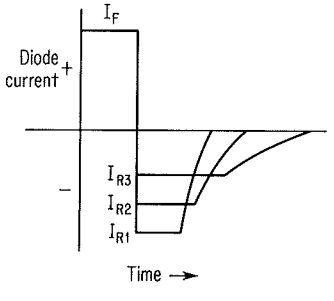


Fig. 10-9. Transient-current response for a diode switched from a constant forward current to three different levels of reverse current.

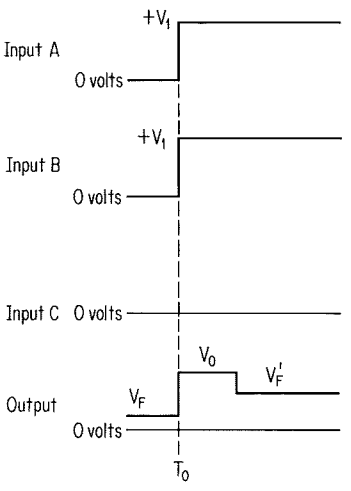


Fig. 10-10. Input- and output-voltage levels for varying signals to inputs A and B in diode AND/OR circuit of Fig. 10-3.

A second type of widely used diode gate is shown in Fig. 10-11. Output voltage at terminal L is clamped to one diode drop *below* the most positive input-signal level. Thus, if input A *or* input B *or* input C is at $+V_1$ volts, the output voltage is at $V_1 - V_F$ volts. For binary 1 equal to a relatively positive-voltage level, the output signal is at binary 1 when at least one input signal is at binary 1. The circuit is an OR gate for positive logic and is represented by the Boolean expression

$$L = A + B + C \qquad (10\text{-}4)$$

where L, A, B, and C are positive-logic binary levels at the respective terminals. On the other hand, output-voltage level of the above diode circuit is relatively negative only when input A *and* input B *and* input C are low (at ground potential). For this reason, the circuit serves as an AND gate for negative logic and can be described by the logical expression

$$L = ABC \qquad (10\text{-}5)$$

where L, A, B, and C are negative-logic binary levels at the respective terminals. Because the diode gate of Fig. 10-11 performs a dual logical operation, the circuit will be referred to as an "OR/AND gate."

An equivalent circuit for the loaded OR/AND diode gate is shown in Fig. 10-12. Capacitance C_0' represents the parallel combination of all diode capacitances, wiring capacitance, and load capacitance. The Thévenin equivalent voltage and resistance values are represented by $-V'$ and R', respectively. Consider that the input signal rises instantaneously from 0 to $+V_1$ volts; C_0' is quickly charged to $V_1 - V_F$ volts by current flow from the input-signal source and through the forward-biased diode. If the input signal decreases instantaneously to 0 volts, C_0' discharges through the current sink consisting of R' and $-V'$. The negative-going edge of the output-voltage waveform is seen to decrease at a rate determined by R', $-V'$, and C_0'.

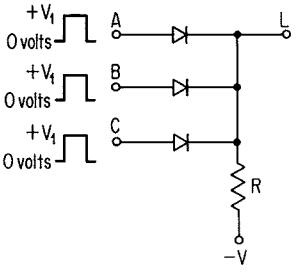


Fig. 10-11. Circuit configuration of OR/AND diode gate.

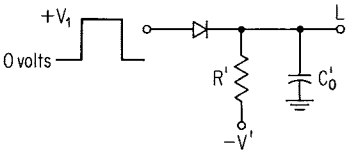


Fig. 10-12. Equivalent circuit of OR/AND diode gate with an external load.

Restrictions exist upon the number of input (fan-in) diodes to each of the above two gate circuits. Equivalent load capacitance is increased for larger values of fan-in, and transient response of the circuit becomes poorer. Diode leakage currents restrict fan-in on the basis of dc considerations insofar as loading of the signal source is concerned.

Various logical combinations of input signals may be formed by cascading the AND/OR and OR/AND diode gates. In order to describe the design of cascade connections of these gates clearly, only positive logic will be considered for the remainder of this section: each gate type will be referred to by its function as a positive logic element. Thus, the AND/OR gate will be designated as an "AND gate" and the OR/AND gate will be referred to as an "OR gate."

A cascade connection of the AND and OR gates is shown in Fig. 10-13. The AND and OR portions of the circuit have fan-in factors of M_1 and M_2, respectively. In order to study the effect of diode-leakage current, consider that the OR-gate inputs to diodes D_5 and D_6 are at ground potential. An equivalent-circuit representation for the above operating conditions is shown in Fig. 10-14. Total diode leakage current is indicated by $(M_2 - 1)I_L$.

When the input signal to the above circuit is at $+V_1$ volts, external-load current I_P, diode-leakage currents $(M_2 - 1)I_L$, and current I_1 into the $-V_3$ supply cause a voltage drop across resistor R_1. In general it is desirable for voltage at node X to be clamped by the input diode to one diode drop above the input-signal level. As output voltage of the circuit is one diode drop *below* the voltage at node X, there will be little shift in signal level through the circuit if the input signal does clamp the voltage at node X. In addition, power supply and resistor values can vary somewhat and yet not significantly change the level of output voltage. Also, voltage to an external load is accurately known, and the effects of various loads can readily be evaluated.

In order to design the above circuit for a clamped voltage at node X, consider that the input diode is temporarily disconnected from the circuit. Voltage at node X is then given by

$$V_X = V_2 - [I_1 + I_P + (M_2 - 1)I_L]R_1 \tag{10-6}$$

Current I_1 is given by

$$I_1 = \frac{V_X - V_F + V_3}{R_2} \tag{10-7}$$

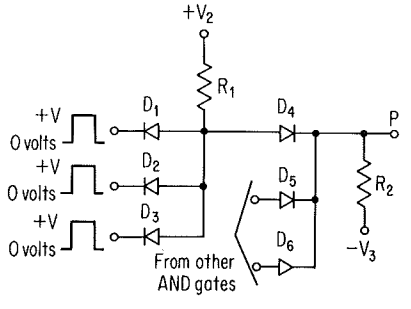


Fig. 10-13. Cascade connection of positive-logic AND and OR gates.

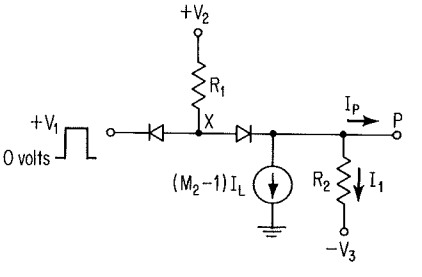


Fig. 10-14. Equivalent-circuit representation of Fig. 10-13 for inputs to D_5 and D_6 at ground potential.

Substitution of the right side of Eq. (10-7) for I_1 in Eq. (10-6) yields

$$V_X = \frac{V_2R_2 - R_1[V_3 - V_F + R_2I_L(M_2 - 1) + R_2I_P]}{R_1 + R_2} \tag{10-8}$$

If the input diode is now connected to the circuit, clamping will occur at node X if $V_X \geqslant V_1 + V_F$. Thus, the right side of Eq. (10-8) should be equal to or greater than the magnitude of $V_1 + V_F$. The following example illustrates a typical design of the AND-OR circuit.

EXAMPLE 10-1

PROBLEM: The input signal to a gate of the type shown in Fig. 10-13 varies from ground potential to +6 volts. The diodes are silicon devices and have 1 μa of leakage current for a reverse bias of 8 volts at 25°C. Suitable resistor and supply-voltage values are to be selected for circuit operation at 25°C. Load current I_P has a value of 3 ma.

SOLUTION: *Step 1.* The positive supply voltage should be considerably larger than the +6-volt input level. A +12-volt level is chosen for the positive supply voltage. For convenience, the negative supply voltage is chosen to be −12 volts.

Step 2. Since V_1 has a magnitude of 6 volts and V_F is equal to approximately 0.7 volt, V_X in Eq. (10-8) is to be larger than 6.7 volts. Let V_X have values of 7.0, 7.5, and 8.0 volts in Eq. (10-8); resulting plots of R_2 versus R_1 are shown in Fig. (10-15) for the three different values of V_X. The V_F term in Eq. (10-8) is considered to have a value of 0.7 volt. A diode-leakage current of 1 μa is used in the calculations. Suitable values of R_1 and R_2, for the desired value of V_X, can be obtained from the above plots.

DISCUSSION: If resistor values are chosen for a V_X of 8.0 volts, the power-supply and resistor levels can vary more than if a lower value of V_X is selected. On the other hand, for a given value of R_2, power dissipation of the circuit is reduced as V_X is made smaller. For any level of V_X, circuit speed and power dissipation increase as R_1 and R_2 are made smaller.

Load current can vary from 0 to 3 ma, and the voltage at node X will remain clamped at the $V_1 + V_F$ level. Output voltage at terminal P is approximately equal to the V_1 level for the above range of load current. A graphical analysis can be used to obtain exact voltage levels in the circuit.

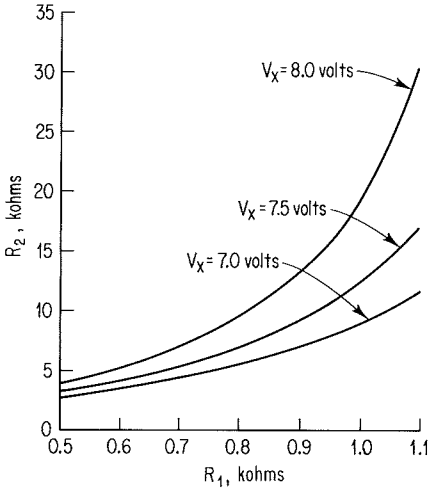


Fig. 10-15. Plots of R_2 and R_1 to give various voltages at node X in Fig. 10-14; input diode is temporarily disconnected.

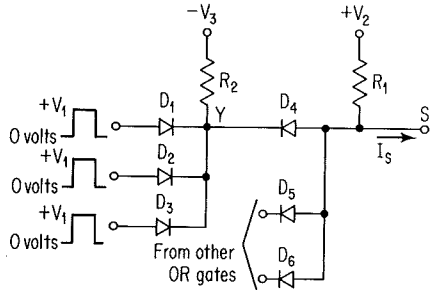


Fig. 10-16. Positive-logic OR gates driving a positive-logic AND gate.

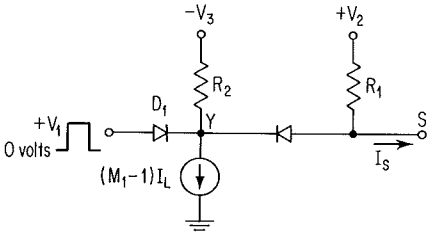


Fig. 10-17. Equivalent-circuit representation of Fig. 10-16 for inputs to D_2 and D_3 at ground potential.

Figure 10-16 shows an OR gate driving an AND gate. The number of fan-in diodes to the OR and AND gates is denoted by M_1 and M_2, respectively; each gate is shown to have a fan-in of 3. Diodes D_4, D_5, and D_6 are each connected to similar OR gates. The AND gate has a positive output level when *each* OR gate has at least one positive input-signal level.

Consider, for purposes of this analysis, that the input-signal levels to D_4, D_5, and D_6 in the above circuit are always identical. Diode reverse-leakage current is most significant when two of the three input diodes to an OR gate have grounded input terminals. The above OR-AND circuit can be replaced by the equivalent circuit shown in Fig. 10-17.

The circuit of Fig. 10-17 is to be designed so that output voltage at terminal S follows closely the circuit input levels of 0 and $+V_1$ volts. This is accomplished by clamping the voltage at node Y to one diode drop *below* the input-signal level; voltage at terminal S is one diode drop *above* the input-voltage level to the AND gate and is approximately equal to the input-signal level to the OR gate.

Consider that diode D_1 is temporarily disconnected from the circuit of Fig. 10-17. Voltage at node Y is given by

$$V_Y = \frac{R_2\{V_2 - [I_S + (M_1 - 1)I_L + I_S]R_1 - V_F\} - V_3R_1}{R_1 + R_2} \qquad (10\text{-}9)$$

If D_1 is now connected to the circuit, node Y is clamped to one diode drop below the input-signal level if $V_Y \leq -V_F$. Further design of the OR-AND circuit can proceed in a manner similar to that described in the foregoing example of AND-OR gate design.

10-3. DIRECT-COUPLED TRANSISTOR LOGIC

In one of the early forms of transistor logic circuit, the collector of an inverter transistor was connected directly to the base of a succeeding stage.[5] This form of transistor logic is referred to as "direct-coupled transistor logic" (DCTL). Although the DCTL configuration is not widely used today, it is discussed here in order to illustrate certain features of subsequent forms of logic circuits.

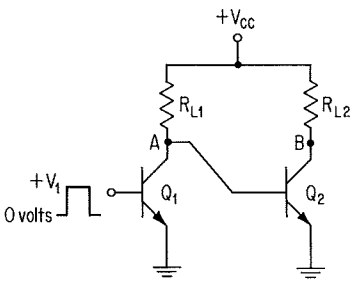


Fig. 10-18. DCTL circuit.

Figure 10-18 shows a DCTL circuit. Consider, for the moment, that the base of transistor Q_2 is not connected to the collector of transistor Q_1 and also that this latter transistor is at collector-current cutoff; collector voltage of Q_1 is close to the V_{CC} level. If the base of Q_2 is now connected to the collector of Q_1, current will flow through R_{L1} into the base of Q_2, and the voltage at point A will fall to the $V_{BE(ON)}$ level of Q_2. Forward base current to Q_2 saturates this device, and the voltage at point B is close to ground potential. When Q_1 is driven to saturation, the voltage at point A becomes equal to the $V_{CE(sat)}$ level of Q_1. If this voltage is less than that required to turn on Q_2, the voltage at point B will rise to nearly the level of V_{CC}.

Transistor logic circuits are generally considered to use the same transistor type in each stage. This practice will be followed throughout the remainder of the present chapter. Hence, the output characteristics of a transistor stage must be compatible with the input characteristics of a succeeding transistor stage employing the *same* transistor type.

Figure 10-19*a* shows a typical curve of I_C versus V_{BE} for a germanium-alloy transistor; collector current is seen to be almost negligible until the base-emitter voltage exceeds about 0.2 volt. A typical family of collector characteristic curves for this transistor is shown in Fig. 10-19*b*; voltage from collector to emitter of the saturated transistor is seen to be less than 0.2 volt. If this particular transistor type is used in the circuit of Fig. 10-18, the $V_{CE(sat)}$ level of Q_1 will prevent Q_2 from turning on, and the circuit will operate satisfactorily. Most switching-type transistors have relative magnitudes of $V_{CE(sat)}$ and $V_{BE(ON)}$ which allow devices of the same type to be used in the above circuit.

Logic can be performed by connecting the collectors of two or more transistors together, as shown in Fig. 10-20. Since transistors Q_1, Q_2, and Q_3 are inverters, a positive-level input signal to either device will cause the voltage level at point D

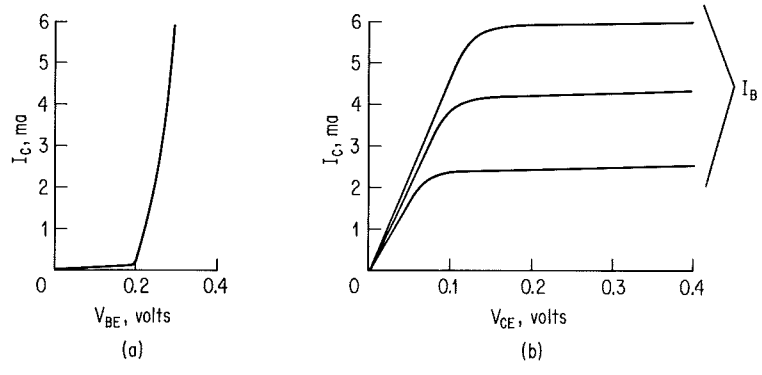


Fig. 10-19. Characteristic curves of germanium-alloy transistor. *(a)* I_C **versus** V_{BE}; *(b)* I_C **versus** V_{CE}.

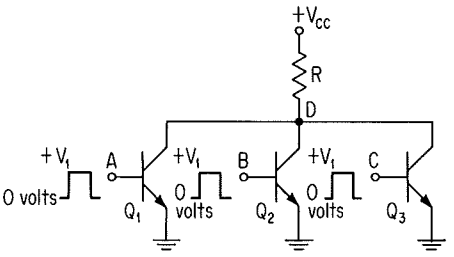


Fig. 10-20. DCTL circuit to perform NOR/NAND logic.

to be relatively negative. Hence, each inverter performs the NOT function upon its own input signal. The parallel collectors perform the OR function for positive logic and the AND function for negative logic. Boolean expressions to define the circuit functions can be written

$$\text{Output} = \overline{A + B + C} \tag{10-10}$$

for a positive-logic system, and

$$\text{Output} = \overline{ABC} \tag{10-11}$$

for a negative-logic system. The above DCTL stage is considered to be a NOR (NOT-OR) gate for positive logic and a NAND (NOT-AND) gate for negative logic. In accordance with the nomenclature established previously, the circuit of Fig. 10-20 is a NOR/NAND gate.

The bases of two or more transistors can be driven from a common point, as shown in Fig. 10-21. Each of these fan-out transistors can be connected, at their collectors, to collectors of other transistors.

Only one supply voltage is normally used for DCTL circuitry. This voltage is typically 1.5 to 3 volts. In the circuit of Fig. 10-21, R_{L1} serves as a load resistor for Q_1 and is also the base-input resistor to Q_2, Q_3, and Q_4. This resistance is large compared to the saturation resistance of a transistor, and it is also much larger than the base-input resistance of a fan-out transistor. The current through R_{L1} can be considered a constant current; this type of logic can be thought of as switching a constant current from the collector of one transistor to the base of one or more fan-out transistors. Because of the small voltage swing at the collector of a DCTL stage (except for the final stage), circuit speed is not seriously deteriorated by the effects of load capacitance.

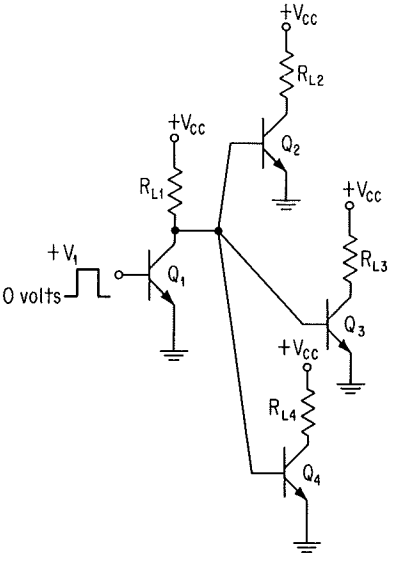


Fig. 10-21. Fan-out loading of a DCTL inverter.

Fan-in and fan-out loadings in DCTL are not independent of each other. Consider that in Fig. 10-22 Q_1 and Q_2 are at cutoff

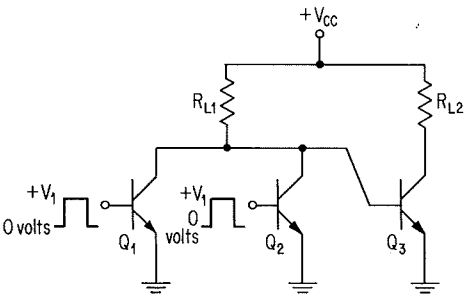
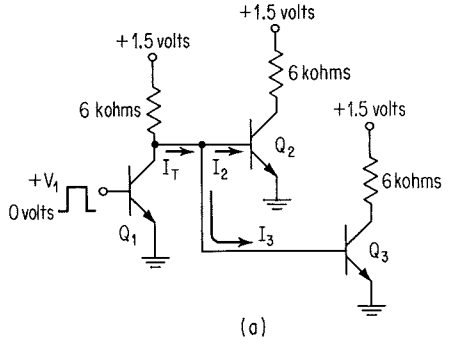


Fig. 10-22. Collector leakage currents of fan-in transistors Q_1 and Q_2 reduce forward base drive to fan-out transistor Q_3.

while Q_3 is in conduction. Base current of Q_3, as well as collector leakage currents of Q_1 and Q_2, must be supplied from the current source consisting of R_{L1} in series with V_{CC}. Collector leakage currents of Q_1 and Q_2 reduce drive current to the base of Q_3. If additional fan-in transistors are added, the total collector leakage current must not be so large that Q_3 will fail to conduct. Additional fan-out transistors can be added to the circuit of Fig. 10-22 only if there is adequate current through R_{L1} to supply the turn-on current of all fan-out transistors and the collector leakage current of all fan-in transistors.

Two unfavorable aspects of circuit operation have prevented the DCTL configuration from becoming widely used. The first of these is the storage-time effect in a DCTL stage. Consider the circuit of Fig. 10-18. Resistors R_{L1} and R_{L2} have the same magnitude, and forward base drive to Q_2 is almost equal to collector current of the device. The resulting large overdrive to Q_2 causes an excessive storage time in this transistor. Although storage time can be minimized by the



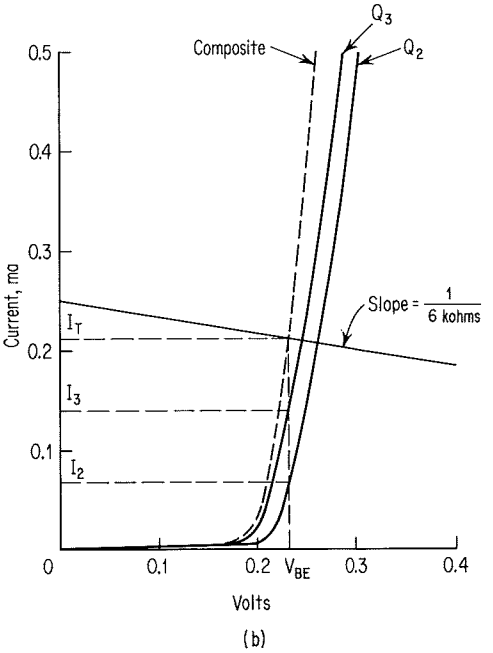


Fig. 10-23. Base-robbing effect in DCTL circuit. *(a)* Fan-out loading of 2; *(b)* graphical analysis to show distribution of base current.

use of diffused-base epitaxial transistors, other logic circuit configurations have been developed which have less of a storage-time problem.

The second major disadvantage of the DCTL circuit is a current "hogging," or "base-robbing," effect. Consider the circuit of Fig. 10-23*a* which has a fan-out of 2. Transistors Q_2 and Q_3 are devices of the same type but have slightly dissimilar I_B versus V_{BE} characteristics. A graphical analysis is performed in Fig. 10-23*b* and shows that Q_3 "hogs" most of the current available from the base-current source. Unless transistor input characteristics are carefully matched, there is a strong possibility that one fan-out transistor may "rob" sufficient base current from the other fan-out devices to prevent them from saturating.

As a practical matter, troubleshooting of a faulty DCTL network can be a time-consuming task. If several transistors are wired together and a short develops in one transistor, it may be necessary to remove each transistor from the circuit in order to test for the shorted device.

10-4. TRANSISTOR-RESISTOR LOGIC

Resistors can be inserted between the collector of a transistor and the bases of fan-out transistors, as shown in Fig. 10-24. These resistors serve to make base current to a transistor relatively independent of the base-emitter diode characteristic of the device. Hence, base currents to Q_2 and Q_3 in the above figure are determined principally by the magnitudes of R_B and R_{L1}. In order to reverse-bias Q_1, Q_2, and Q_3 in the OFF state and also to provide a sink for collector-base leakage currents of these devices, resistor R_K and supply voltage $-V_{BB}$ can be added to the inputs, as shown in Fig. 10-25.[6] This latter circuit is generally referred to as either a "transistor-resistor logic" (TRL) stage, or as a "resistor-transistor logic" (RTL) stage. The former circuit designation will be used in this discussion.

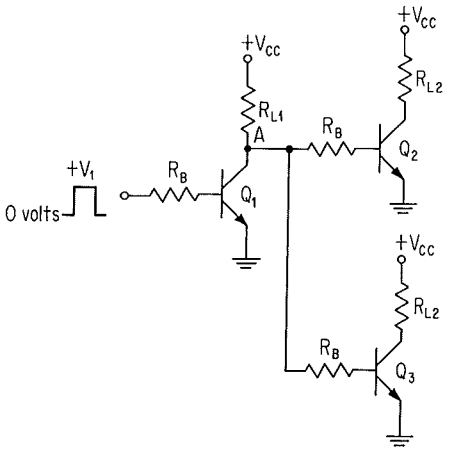


Fig. 10-24. Base-input resistors to Q_2 and Q_3 provide more uniform distribution of base current from point A.

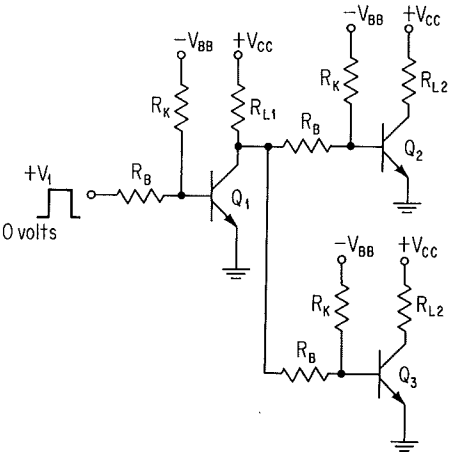


Fig. 10-25. TRL stages.

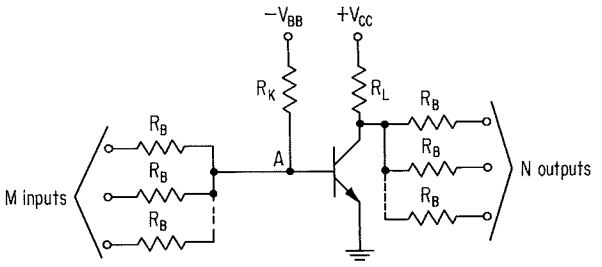


Fig. 10-26. General circuit configuration for TRL.

A general circuit configuration for the TRL stage is shown in Fig. 10-26. The M fan-in resistors are connected to collectors of preceding stages. The collector fans out to N base-input resistors. When all input signals are at ground potential, the TRL circuit can be represented as shown in Fig. 10-27*a*.* Voltage at point A is given by

$$V_A = \frac{-R_B(V_{BB} - R_K I_{BX})}{MR_K + R_B} \tag{10-12}$$

If any input signal to the above TRL stage rises to $+V_1$ volts, current flows from the signal source, through an input resistor, and into node A. Figure 10-27*b* shows the TRL circuit for one input signal at $+V_1$ volts. The input resistors connected to ground potential are in parallel with each other and are represented by resistance $R_B/(M-1)$. Output loading is represented by resistance R_B/N; current I_L flows through this resistance as shown. Base current to the transistor can be described by

$$I_B = I_1 - I_2 - I_3 \tag{10-13}$$

Individual expressions can be written for I_1, I_2, and I_3 and substituted into Eq. (10-13); this gives

*For simplicity, the input-signal levels are presently considered to vary between ground potential and $+V_1$ volts.

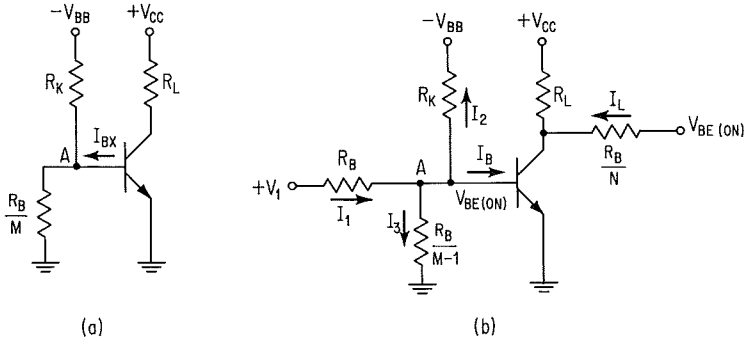


Fig. 10-27. Equivalent circuits for TRL stage. *(a)* **All input signals at ground potential;** *(b)* **one input signal at $+V_1$ volts.**

$$I_B = \frac{V_1 - MV_{BE(ON)}}{R_B} - \frac{V_{BB} + V_{BE(ON)}}{R_K} \tag{10-14}$$

Base current determined from the above expression must be at least as large as the minimum value required to saturate the transistor; this minimum base current is given by

$$I_{B(min)} = \frac{V_{CC} - V_{CE(sat)}}{h_{FE}R_L} + \frac{(V_{BE(ON)} - V_{CE(sat)})N}{R_B} \tag{10-15}$$

Forward base current to the TRL stage is determined by the number of input signals. For a stage having a fan-in of M, base turn-on current may be as low as that given by Eq. (10-14); however, this current would be considerably larger if all inputs were energized. The lowest value of forward base current results in a maximum turn-on time for the transistor. Maximum turnoff time occurs when there is a maximum value of forward base current.

The transistor in a TRL circuit inverts the signal which appears at the common junction of the input resistors and hence performs the NOT operation upon this signal. Input resistors of the circuit perform the OR function for positive logic and the AND function for negative logic. The TRL stage performs the same logic function as the DCTL stage of Fig. 10-19 and consequently can be described by Eqs. (10-10) and (10-11). The TRL stage is considered to be a NOR/NAND gate.

Combinations of TRL stages can be used to perform any desired logic operation. Consider the OR and AND operations in a positive-logic system. The NOR output of a TRL stage can be inverted by a single-input TRL gate to give the OR function. From Eq. (9-21), it is seen that an AND operation is equivalent to the OR operation upon the complements of the various variables. Hence, if complementary inputs are applied to the NOR gate, the output will be the NOR grouping of these complementary variables and consequently will be the AND grouping for the true variables.

Worst-case Design. A TRL gate is driven by M input stages and, in turn, serves as one driver for N output stages. Expressions for turn-on base current and reverse-bias voltage to the transistor depend upon values of M (fan-in) and N (fan-out), in addition to resistance and supply-voltage values. One common method of designing a TRL stage is to use a "worst-case" design procedure. Equations are written for the ON and OFF states of the TRL stage under the conditions that all circuit parameters are at their extreme limits, which would tend to make the circuit inoperative. The ON and OFF expressions are solved for a minimum value and a maximum value, respectively, for R_B. Following this, plots are made of $R_{B(min)}$ and $R_{B(max)}$ versus nominal values of R_K for all circuit parameters at their worst-case levels. Any value of R_B lying above the $R_{B(min)}$ plot and below the $R_{B(max)}$ plot, together with the corresponding value of R_K, allows the TRL stage to function properly. This method of selecting resistance values from plotted curves is similar to that described in Example 6-3, but worst-case design was not considered in that example.

In Fig. 10-28*a*, transistor Q_2 has a fan-in of M and a fan-out of N. A single OFF

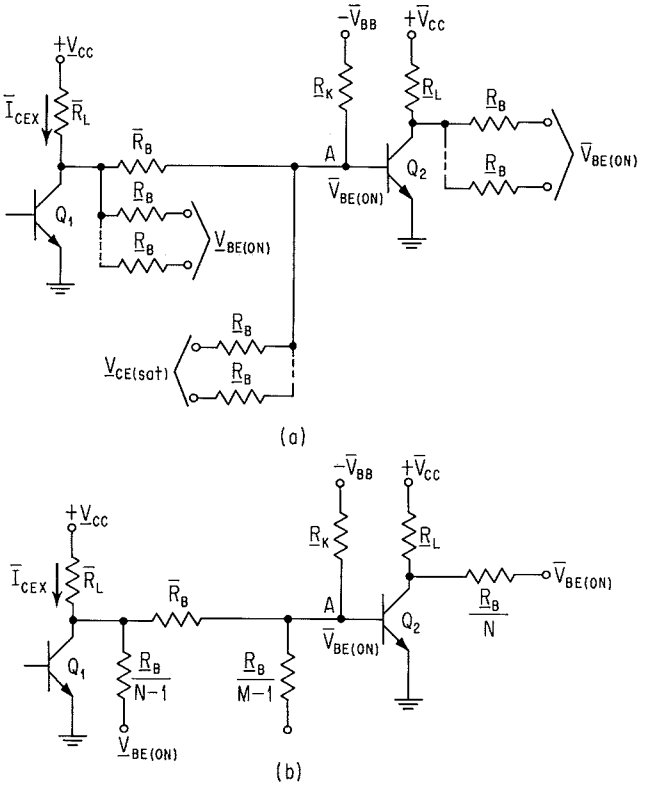


Fig. 10-28. Worst-case ON conditions for TRL stage. *(a)* **Complete circuit;** *(b)* **equivalent circuit.**

transistor Q_1 provides forward base drive to Q_2. Each circuit parameter is shown to have a maximum value (a line over the first letter in the symbol) or a minimum value (a line under the first letter in the symbol). Each parameter is at the limit which would tend to prevent Q_2 from saturating. For instance, although Q_1 is at cutoff, maximum leakage current for this transistor, in addition to a maximum value of R_L and a minimum value of V_{CC} to Q_1, causes a minimum current to flow into node A. All circuit parameters are at their worst-case values. It will be noticed that V_{CC} is shown to have a minimum value in conjunction with Q_1 and a maximum value in conjunction with Q_2. Although this situation cannot physically exist, the design analysis will employ the two different values of V_{CC}. This affords an even more conservative design than if V_{CC} were chosen at either a minimum or a maximum value. Figure 10-28*b* shows an equivalent representation of the above TRL stage. Minimum forward base current to Q_2 can be written

$$I_B = \frac{(\underline{V}_{CC} - \bar{I}_{CEX}\bar{R}_L - \bar{V}_{BE(ON)})\underline{R}_B + \bar{R}_L(N-1)(\underline{V}_{BE(ON)} - \bar{V}_{BE(ON)})}{\bar{R}_L\underline{R}_B + \bar{R}_B\bar{R}_L(N-1) + \underline{R}_B\bar{R}_B} - \frac{(\bar{V}_{BE(ON)} - \underline{V}_{CE(sat)})(M-1)}{\underline{R}_B} - \frac{\bar{V}_{BB} + \bar{V}_{BE(ON)}}{\underline{R}_K} \qquad (10\text{-}16)$$

Maximum collector current of Q_2 can be described by

$$\bar{I}_C = \frac{\bar{V}_{CC} - \underline{V}_{CE(\text{sat})}}{\underline{R}_L} + \frac{(\bar{V}_{BE(\text{ON})} - \underline{V}_{CE(\text{sat})})N}{\underline{R}_B} \tag{10-17}$$

For h_{FE} of Q_2 at a minimum value, the minimum required base current is given by

$$\underline{I}_B = \frac{\bar{I}_C}{\underline{h}_{FE}} \tag{10-18}$$

The right side of Eqs. (10-16) and (10-17) can be substituted into Eq. (10-18) and the resulting expression solved for R_K; this yields

$$R_K = \frac{\bar{V}_{BB} + \bar{V}_{BE(\text{ON})}}{\dfrac{(\underline{V}_{CC} - I_{CEX}\bar{R}_L - \bar{V}_{BE(\text{ON})})\underline{R}_B + \bar{R}_L(N-1)(\underline{V}_{BE(\text{ON})} - \bar{V}_{BE(\text{ON})}}{\bar{R}_L\underline{R}_B + \bar{R}_B\bar{R}_L(N-1) + \underline{R}_B\bar{R}_B} - \dfrac{(\bar{V}_{BE(\text{ON})} - \underline{V}_{CE(\text{sat})})(M-1)}{\underline{R}_B} - \dfrac{[\underline{R}_B(\bar{V}_{CC} - \underline{V}_{CE(\text{sat})}) + \bar{R}_L(\bar{V}_{BE(\text{ON})} - \underline{V}_{CE(\text{sat})})N]}{\underline{h}_{FE}\bar{R}_L\underline{R}_B}} \tag{10-19}$$

Worst-case conditions are shown in Fig. 10-29*a* for the TRL stage at cutoff. An equivalent circuit for this cutoff condition is shown in Fig. 10-29*b*; from this figure,

$$\bar{I}_1 = \frac{(V_{BE(\text{OFF})} + \bar{V}_{CE(\text{sat})})M}{\underline{R}_B} \tag{10-20}$$

and

$$\underline{I}_2 = \frac{\underline{V}_{BB} - V_{BE(\text{OFF})}}{\bar{R}_K} \tag{10-21}$$

Currents at node A can be summed to give

$$\underline{I}_2 = \bar{I}_1 + \bar{I}_{BX} \tag{10-22}$$

The right side of Eqs. (10-20) and (10-21) can be substituted into Eq. (10-22); this gives, after slight rearrangement of terms,

$$\bar{R}_K = \frac{\underline{V}_{BB} - V_{BE(\text{OFF})}}{[(V_{BE(\text{OFF})} + \bar{V}_{CE(\text{sat})})M]/\underline{R}_B + \bar{I}_{BX}} \tag{10-23}$$

A nominal value of $V_{BE(\text{OFF})}$ is used in the above expressions. Equation (10-23)

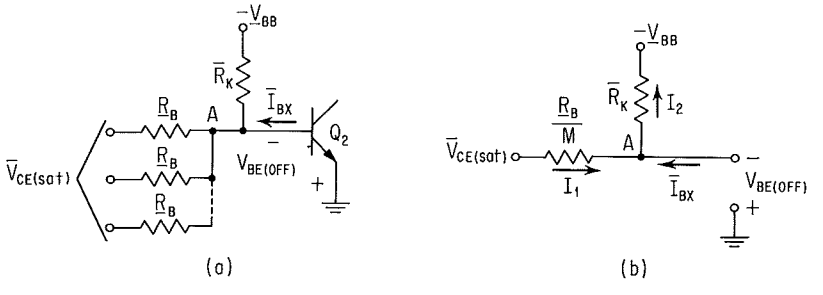


Fig. 10-29. Worst-case OFF conditions for TRL stage. *(a)* **Complete circuit;** *(b)* **equivalent circuit.**

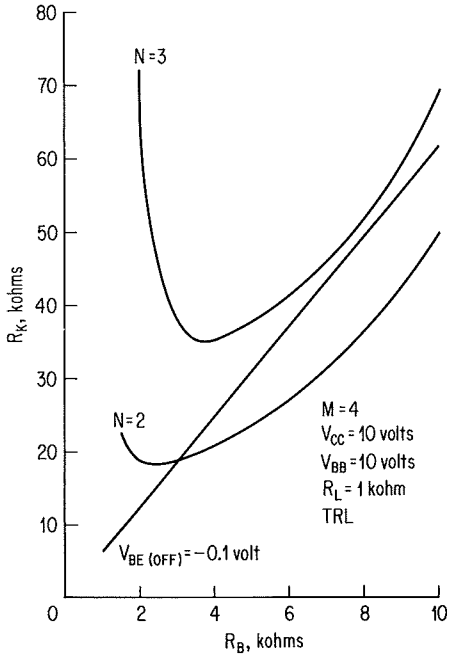


Fig. 10-30. Plots of R_K versus R_B for two values of fan-out.

determines the maximum value of R_K which will permit the $V_{BE(OFF)}$ level to be as large as the desired value.

Plots of R_K versus R_B are given in Fig. 10-30 for a TRL stage having a fan-in of 4; ambient temperature is at the 25°C level. The N-P-N transistor has the following characteristics:

$$\begin{aligned}
\bar{V}_{BE(ON)} &= 0.85 \text{ volt} \quad @ \quad I_C = 10 \text{ ma}, I_B = 0.6 \text{ ma} \\
\underline{V}_{BE(ON)} &= 0.80 \text{ volt} \quad @ \quad I_C = 10 \text{ ma}, I_B = 0.5 \text{ ma} \\
\bar{V}_{CE(sat)} &= 0.25 \text{ volt} \quad @ \quad I_C = 10 \text{ ma}, I_B = 0.6 \text{ ma} \\
\underline{V}_{CE(sat)} &= 0.20 \text{ volt} \quad @ \quad I_C = 10 \text{ ma}, I_B = 0.5 \text{ ma} \\
\bar{I}_{CEX} &= 1 \ \mu\text{a} \quad @ \quad V_{BE(OFF)} = 1.5 \text{ volts}, V_{CC} = 10 \text{ volts} \\
\bar{I}_{BX} &= 2 \ \mu\text{a} \quad @ \quad V_{BE(OFF)} = 1.5 \text{ volts}, V_{CC} = 10 \text{ volts} \\
h_{FE} &= 50 \quad @ \quad I_C = 10 \text{ ma}, \quad V_{CE} = 1 \text{ volt}
\end{aligned}$$

Nominal values of V_{BB} and V_{CC} are -10 and $+10$ volts, respectively. A power-supply variation of ± 2 per cent and a resistance variation of ± 10 per cent are assumed. The load resistor has a nominal value of 1.0 kilohm. Equation (10-23) is plotted for a $V_{BE(OFF)}$ of -0.1 volt, and Eq. (10-19) is plotted for two different values of N. The plots show that the area of solution decreases as N is made larger.

If it is desired to operate a TRL stage over a range of ambient temperatures, the ON and OFF equations should be plotted for the two temperature extremes. The smaller area of solution should be used for selection of component values.

For any operating temperature, the area of solution will be increased for one or more of the following circuit changes:

1. Decrease value of M.
2. Decrease per cent variation of R_K.
3. Decrease per cent variation of R_B.
4. Decrease per cent variation of V_{BB}.
5. Decrease per cent variation of V_{CC}.
6. Decrease value of $V_{BE(\text{OFF})}$.

Worst-case design gives a circuit which will operate satisfactorily under the adverse circuit conditions considered in the design procedure. However, the conservative nature of worst-case design is often a reason for not using this design technique. For instance, the plots of R_K versus R_B in Fig. 10-30 show that under worst-case conditions, the circuit cannot have a fan-in of 4 and a fan-out of 3. Suppose, however, that it would be highly desirable to have circuits with the above values of M and N. What can be done? Tighter-tolerance resistors can be used, per cent variation of power-supply voltages can be reduced, and a higher-gain transistor can be employed. But these "improvements" in circuit parameters increase the cost of the circuit. On the other hand, if nominal values of all parameters were used in the ON and OFF equations, an area of solution would be found for $M = 4$ and for $N = 3$. Because there is only a small probability that *all* circuit parameters will go to their extreme values simultaneously, worst-case design is overly conservative. Yet, it is not reasonable to consider that all parameters will be at their nominal values. What is required is a design procedure which is not so conservative as worst-case design but which will yield a suitable circuit. The following section describes a design technique which can meet the above requirements.

10-5. STATISTICAL DESIGN

It was pointed out in the foregoing section that because all circuit parameters do not simultaneously go to their extreme values, worst-case circuit design is unduly conservative. The alternate method of circuit design presented here can best be described as a simulation process. Simply stated, many different transistor parameters and component values are assumed, and calculations are made to determine whether the circuit will operate satisfactorily. In this manner, thousands of circuits can be simulated and the circuit "yield" can be determined. The simulation process is illustrated below for design of a NOR/NAND gate of the type shown in Fig. 10-26. This process can be applied to the design of any circuit.

Instead of worst-case values of circuit parameters, actual distributions of circuit parameters are used in the following circuit design. Figure 10-31 shows a typical production distribution of 1,000 resistors which are intended to be at a nominal resistance of R_0 ohms. Many of the resistors have values which are below or above the R_0 level. Actually, there may be no resistor which is exactly at the R_0 level. All circuit parameters have distributions of the type shown in the figure. These distributions may be broad or narrow, depending upon the tolerance assigned to each parameter.

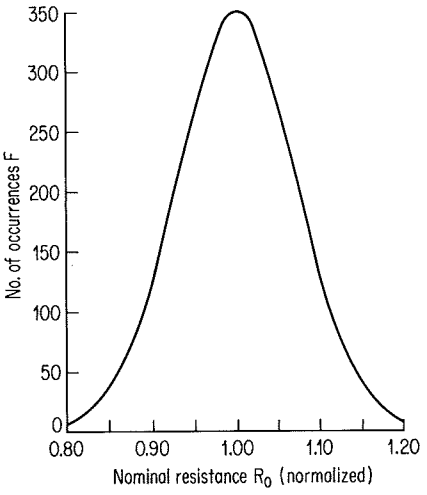


Fig. 10-31. Typical production distribution of 1,000 resistors.

Consider now the TRL circuit of Fig. 10-28*a*. Equation (10-19), which gave the minimum value of R_K in terms of worst-case extremes for all circuit parameters, is rewritten below for nominal values of parameters

$$R_K \geqslant \frac{V_{BB}+V_{BE(\mathrm{ON})}}{\dfrac{V_{CC}-I_{CEX}R_L-V_{BE(\mathrm{ON})}}{R_LN+R_B} - \dfrac{(V_{BE(\mathrm{ON})}-V_{CE(\mathrm{sat})})(M-1)}{R_B} - \dfrac{R_B(V_{CC}-V_{CE(\mathrm{sat})})+R_L(V_{BE(\mathrm{ON})}-V_{CE(\mathrm{sat})})N}{h_{FE}R_LR_B}} \tag{10-24}$$

In a similar manner, an expression for the maximum value of R_K can be obtained by substituting nominal values of parameters into Eq. (10-23); this yields

$$R_K \leqslant \frac{V_{BB} - V_{BE(\mathrm{OFF})}}{[(V_{BE(\mathrm{OFF})} + V_{CE(\mathrm{sat})})M]/R_B + I_{BX}} \tag{10-25}$$

Equations (10-24) and (10-25) can now be used to obtain an area of solution for R_K and R_B; this area is larger than that obtained from a worst-case design.

Various combinations of R_K and R_B are now known which will give a suitable circuit, *provided* that all circuit parameters remain at their nominal values. It is next necessary to select particular values of R_K and R_B and to determine whether the circuit will continue to perform satisfactorily for random variations of the parameters. In order to allow for the widest variation of parameters, let R_K and R_B be chosen from the center of the area of solution.

It is necessary to evaluate the effect of each parameter upon circuit performance. Figure 10-32 gives a circuit which shows conditions of minimum base drive to the TRL stage for nominal values of circuit parameters. Parameters which appear more than once (except for V_{CC}, which is common) are given numerical subscripts. For convenience, the ON subscript is left off the symbol for base-emitter voltage and the sat subscript is left off the symbol for collector saturation voltage. The subscripted variables of the above figure can be substituted into Eq. (10-16) to yield

$$I_B = \frac{(V_{CC} - I_{CEX}R_{L1} - V_{BE2})R_{B1} + R_{L1}(N-1)(V_{BE1} - V_{BE2})}{R_{L1}R_{B1} + R_{B2}R_{L1}(N-1) + R_{B2}R_{B1}} - \frac{(V_{BE2} - V_{CE1})(M-1)}{R_{B2}} - \frac{V_{BB} + V_{BE2}}{R_K} \quad (10\text{-}26)$$

This expression shows the effect of each parameter upon base current. Equation (10-17) gives maximum collector current for the worst-case design analysis; it can be modified for the parameters shown in Fig. 10-23 to yield

$$I_C = \frac{V_{CC} - V_{CE2}}{R_{L2}} + \frac{(V_{BE3} - V_{CE2})N}{R_{B4}} \quad (10\text{-}27)$$

For any saturated-transistor stage

$$I_B h_{FE} \geqslant I_C \quad (10\text{-}28)$$

The above inequality states that the base current determined from Eq. (10-26), times the h_{FE} of the transistor, must be at least as large as the collector current of the device.

Because there was an area of solution for the circuit under discussion, substitution of nominal values of parameters into Eqs. (10-26) and (10-27) will allow the inequality of Eq. (10-28) to be satisfied. What is now required is to vary all parameters, with each parameter taking on many different values, and to determine whether or not the inequality of Eq. (10-28) exists for each combination of parameters. This process of *permuting* each parameter is readily accomplished with the aid of a digital computer. Several hundreds, or even thousands, of circuits can be simulated, and the percentage of usable circuits can be determined. If it is decided that too large a number of the resulting circuits would not give satisfactory operation, restrictions can be put on the allowable values of any, or all, parameters. Thus, the TRL stage can be designed without actually fabricating any circuits.

It is most practical to permute only one parameter at a time. The values which a parameter can assume are determined by the distribution for that parameter. For instance, consider a distribution of base-emitter voltage for 500 transistors, as shown in Fig. 10-33. The nominal value of V_{BE} is at the peak of the distribu-

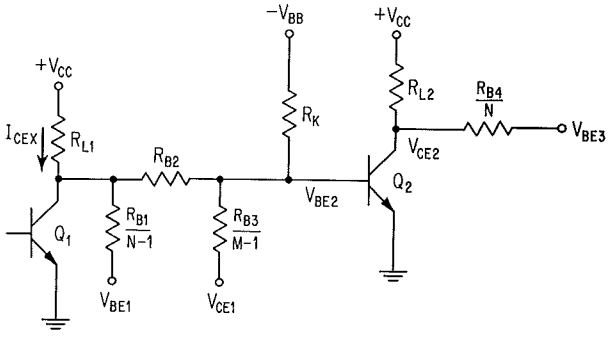


Fig. 10-32. Minimum base drive to Q_2 for nominal values of parameters.

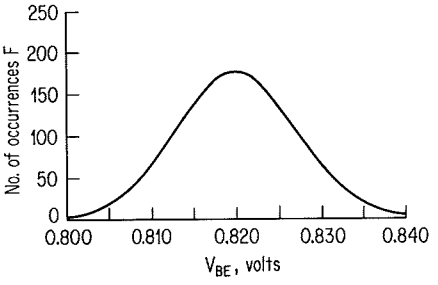


Fig. 10-33. V_{BE} **distribution of 500 transistors.**

tion, or 0.820 volt. The probability of occurrence of V_{BE} can be obtained from the above curve and the relationship

$$P = \frac{F}{N} \tag{10-29}$$

where P = probability of occurrence
F = number of occurrences
N = number of samples (500 in this instance)

Dividing the vertical axis of Fig. 10-33 by N gives a probability curve for the distribution of V_{BE}; Fig. 10-34 shows this probability curve.

Various values of the above probability distribution are to be used for each of the V_{BE} terms in Eqs. (10-26) and (10-27). Consider that V_{BE2} in Eq. (10-26) is permuted first, with all other parameters in the equation at their nominal values. Also, let all parameters in Eqs. (10-27) and (10-28) be at their nominal values. For the present discussion, let the V_{BE} distribution be divided into eight increments, as shown in Fig. 10-34. Also, let it be assumed that calculated results show that the inequality of Eq. (10-28) does not exist for $V_{BE2} \geqslant 0.830$ volt. Hence, it is found that out of nine possible values for V_{BE2}, three will not yield a suitable circuit. However, as the distribution shows that not all values of V_{BE} are equally likely, it is not valid to consider that the circuit yield is 66 per cent. A weighting factor must be assigned to each trial as well as to each satisfactory result. This weighting factor is the probability of occurrence P for the particular value of the parameter. Each "yes" or "no" answer to the inequality of Eq. (10-28) is given the number 1 or 0, respectively; each 1 number is multiplied by the above weighting factor. Table 10-1 shows this for the circuit under discussion.

Individual totals are taken for the P and $P \times Q$ columns in Table 10-1. The ratio of $\Sigma(P \times Q)$ to ΣP shows the weighted number of acceptable circuits

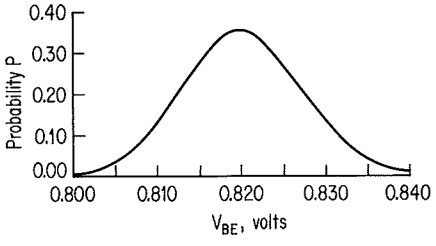


Fig. 10-34. Probability of occurrence for V_{BE}.

Table 10-1. Assignment of Weighting Factor to Trial Calculations

Value of V_{BE}	Probability of occurrence P	Validity Q of Eq. (10-28)	$P \times Q$
0.800	0.0064	1	0.0064
0.805	0.0371	1	0.0371
0.810	0.1288	1	0.1288
0.815	0.2725	1	0.2725
0.820	0.3500	1	0.3500
0.825	0.2725	1	0.2725
0.830	0.1288	0	0.0000
0.835	0.0371	0	0.0000
0.840	0.0064	0	0.0000
	$\Sigma P = 1.2396$		$\Sigma(P \times Q) = 1.0873$

divided by the weighted number of possible circuits and indicates the circuit yield. A yield of 87.7 per cent is obtained for the circuit under consideration.

A method of determining circuit yield with respect to a single parameter is described above. The actual circuit yield is probably slightly higher than the calculated value, as it is not known whether the circuit will function for V_{BE} greater than 0.825 volt but less than 0.830 volt. The calculated yield can be made more accurate by dividing the distribution into a larger number of increments.

This process of permuting a single variable can be repeated for each of the parameters in Eqs. (10-26) to (10-28). If circuit yield for the nth permutation is denoted by U_n, the *total* circuit yield is described by

$$\text{Circuit yield} = U_1 U_2 \cdots U_{n-1} U_n U_{n+1} \cdots \tag{10-30}$$

The foregoing method of simulation is a useful tool in circuit design. This procedure can be applied to any form of circuit. In order to employ this design method successfully, a considerable amount of information must be available concerning the various parameters. In addition, access to a digital computer is an obvious necessity.

10-6. RESISTOR-CAPACITOR-TRANSISTOR LOGIC

Base speedup capacitors can be connected across each of the R_B resistors in Fig. 10-25. A logic circuit of this type is often referred to as a "resistor-capacitor-transistor logic" (RCTL) circuit. The discussion of Sec. 6-7 pointed out that a base speedup capacitor improves transient response of an inverter stage. Care must be taken, however, to assure that capacitive loading does not severely restrict turnoff time of an inverter. The same dc considerations apply to both the TRL and RCTL circuits.

10-7. DIODE-TRANSISTOR LOGIC

The diode logic circuits described in Sec. 10-2 can be combined with transistors to form "diode-transistor logic" (DTL) circuits. In effect, the output of a diode gate is applied to the base of a grounded-emitter transistor; the transistor amplifies the signal and shifts it to the proper voltage level for driving a succeeding stage.

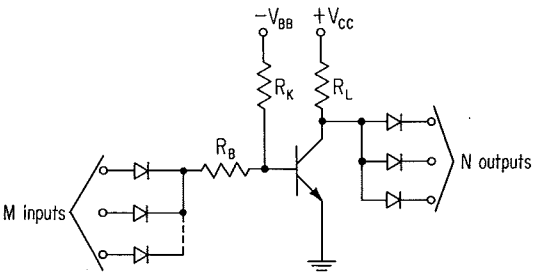


Fig. 10-35. NOR/NAND DTL stage.

Both the OR/AND and AND/OR diode gates can be combined with the transistor; the base input-voltage level to the transistor is inverted, and the complete circuit function is the inverse of that for the diode gate alone. Hence, the OR/AND gate is transformed to a NOR/NAND circuit, and the AND/OR gate becomes a NAND/NOR gate.

NOR/NAND DTL Circuit. Figure 10-35 shows a NOR/NAND DTL stage.[7] A diode OR/AND gate is connected to the input of a single-transistor inverter. When the transistor is at cutoff, resistance R_L and supply voltage V_{CC} serve as a current source to N fan-out transistors. Resistor R_B is connected in series with the transistor base to give an equal distribution of forward base current to the various fan-out transistors connected to a single inverter; this prevents the current-hogging effect. Logic expressions for the above DTL circuit are identical to those for the TRL stage.

Figure 10-36 shows worst-case ON conditions for the DTL stage under discus-

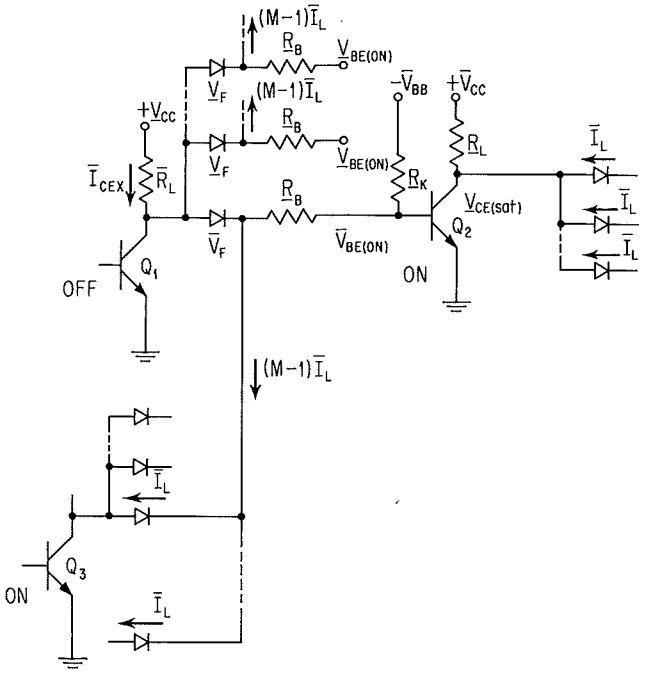


Fig. 10-36. Worst-case ON conditions for NOR/NAND DTL stage.

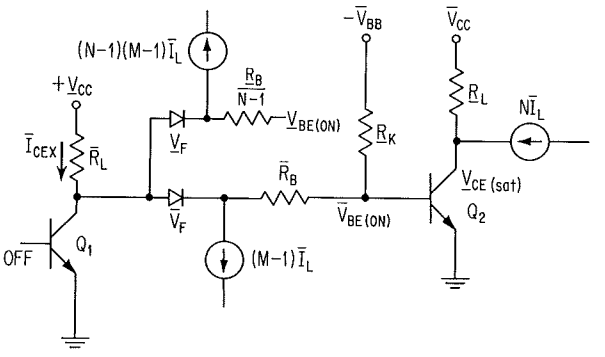


Fig. 10-37. Equivalent circuit for DTL network of Fig. 10-36.

sion. When transistor Q_1 is off, $\bar{R}_L$ in series with $\underline{V}_{CC}$ serves as a current source to turn on N fan-out transistors; in addition, this current source must supply leakage currents to Q_1 and to $M - 1$ reverse-biased diodes. An equivalent circuit for this worst-case condition is given in Fig. 10-37. From this figure, the following expression can be written for a minimum value of R_K

$$\underline{R}_K = \frac{\bar{V}_{BB} + \bar{V}_{BE}}{\dfrac{\bar{R}_L(N-1)(\underline{V}_{BE(ON)} + \underline{V}_F - \bar{V}_{BE(ON)} - \bar{V}_F) + \underline{R}_B\{\underline{V}_{CC} - \bar{V}_F - \bar{V}_{BE(ON)} - \bar{R}_L[\bar{I}_{CEX} + N(M-1)\bar{I}_L]\}}{\underline{R}_B\bar{R}_B + (N-1)\bar{R}_L\bar{R}_B + \bar{R}_L\underline{R}_B} - \frac{1}{\underline{h}_{FE}}\left(\frac{\bar{V}_{CC} - \underline{V}_{CE(sat)}}{\underline{R}_L} + N\bar{I}_L\right)} \tag{10-31}$$

Worst-case OFF conditions for the above DTL stage are shown in Fig. 10-38. An expression for the maximum value of R_K is determined to be

$$\bar{R}_K = \frac{\underline{V}_{BB} - V_{BE(OFF)}}{(V_{BE(OFF)} + \bar{V}_{CE(sat)} - \underline{V}_F)/\underline{R}_B + \bar{I}_{BX}} \tag{10-32}$$

Larger levels of fan-in and fan-out can be obtained with the above DTL configuration than with TRL circuitry. This is seen from plots of R_K versus R_B for the worst-case ON and OFF conditions of the NOR/NAND DTL circuit. Figure 10-39 shows these calculated plots for a DTL stage having a fan-in of 4; the same transistor characteristics, power-supply voltages, load resistances, and resistor and power-supply tolerances are used as for the TRL plots in Fig. 10-30. Diodes in the DTL stage are considered to have a maximum forward-voltage drop of 0.8 volt, a minimum forward-voltage drop of 0.3 volt, and a reverse-leakage current of 1 μa. A comparison of Figs. 10-39 and 10-30 shows that for the same values of fan-in and $V_{BE(OFF)}$, the DTL stage permits a considerably larger fan-out than that of the TRL stage.

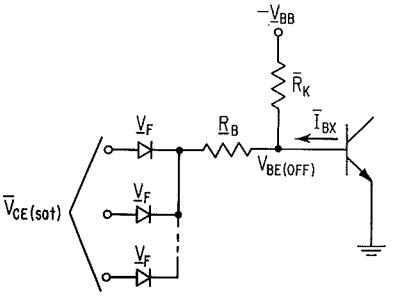


Fig. 10-38. Worst-case OFF conditions for NOR/NAND DTL stage.

Diode recovery time is of concern in the DTL NOR/NAND stage.[7] Consider that all input diodes in the circuit of Fig. 10-35 are forward-biased; current flows through each of these diodes into the transistor base. If the

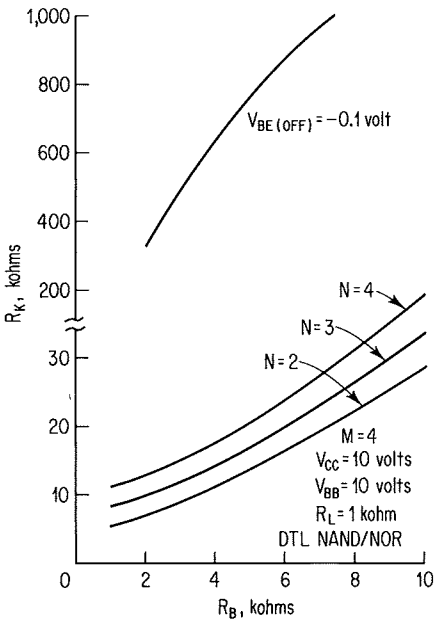


Fig. 10-39. Plots of R_K versus R_B for three values of fan-out.

input signals to two of the diodes are suddenly switched from a positive level to ground potential, reverse-current flow through these two diodes reduces forward base current to the transistor. If the reduction in base current is sufficiently large, the transistor will turn off until the reverse-biased diodes recover.

DTL NAND/NOR Circuits. The AND/OR diode gate can be connected to the input of an inverter to give a NAND/NOR logic stage; this type of circuit is shown in Fig. 10-40.[8] Resistors R_B and R_K, together with the $-V_{BB}$ supply voltage, are included to increase OFF-state noise margin of the circuit. For all diode inputs at ground potential, the voltage at point A is equal to approximately 0.7 volt (for silicon diodes at the input). This voltage level is sufficiently positive to turn on a germanium transistor and to partially turn on a silicon transistor. Current flow into the $-V_{BB}$ supply causes a voltage drop across R_B, and base voltage of the transistor is less positive than the voltage level at point A. Of course, the positive-level input signal to a diode must now be larger than if R_B were shorted, as the voltage drop across this resistor reduces forward base drive to the transistor. The fan-out diodes connected to the collector of Q_1 serve as inputs to succeeding stages.

Forward base drive to the above NAND/NOR logic circuit is provided by the

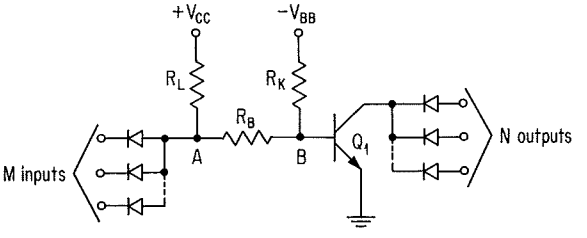


Fig. 10-40. DTL NAND/NOR gate.

current source consisting of R_L in series with V_{CC}. As only one current source connects to the transistor base, forward base current is always at the same level, regardless of the number of input diodes (neglecting leakage currents). The present DTL circuit has no counterpart in the DCTL or TRL configurations.

Worst-case ON and OFF equations are readily determined for the above NAND/NOR circuit. Figure 10-41 shows a worst-case ON condition for this stage; an expression for the minimum value of R_K can be written

$$\underline{R}_K = \frac{\overline{V}_{BB}+\overline{V}_{BE(ON)}}{\dfrac{\underline{V}_{CC}-\overline{R}_L M[\overline{I}_{CEX}+(N-1)\overline{I}_L]-\overline{V}_{BE(ON)}}{\overline{R}_L+\overline{R}_B} - \dfrac{N}{\underline{h}_{FE}}\left[\dfrac{\overline{V}_{CC}-\underline{V}_{CE(sat)}-\underline{V}_F}{\underline{R}_L} + (M-1)\overline{I}_L - \dfrac{\underline{V}_{CE(sat)}+\underline{V}_F+V_{BE(OFF)}}{\overline{R}_B}\right]} \tag{10-33}$$

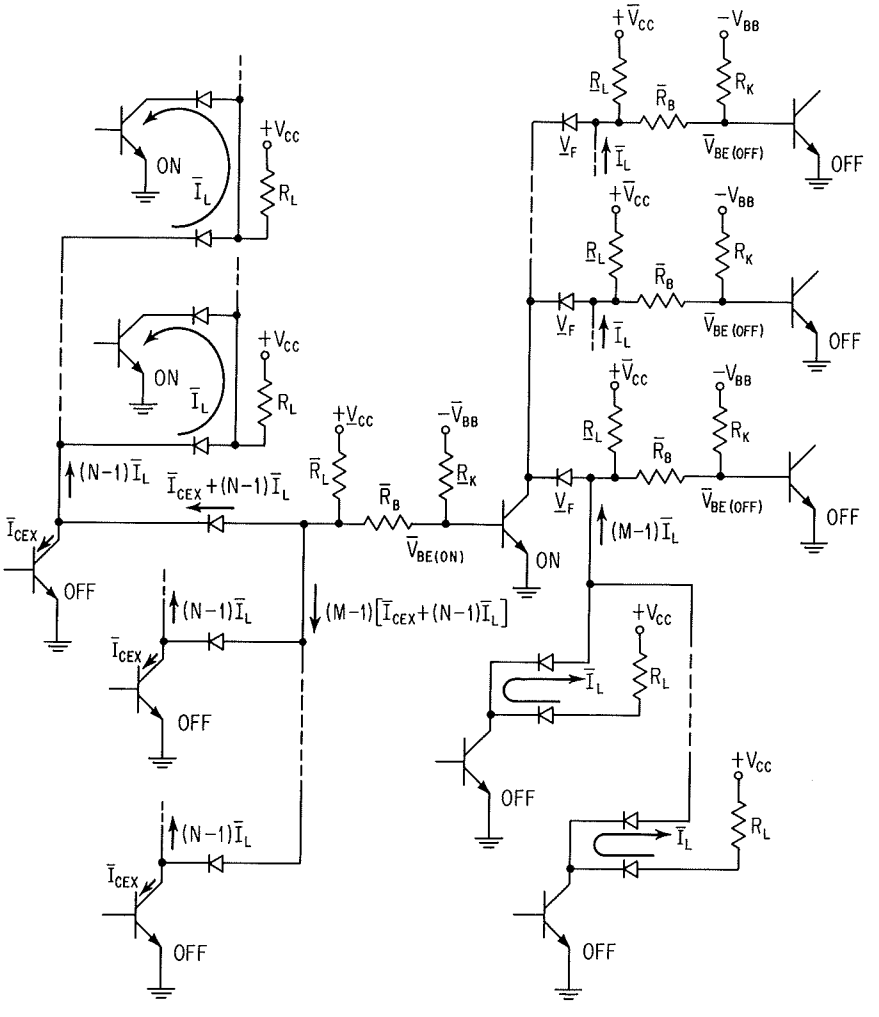


Fig. 10-41. Worst-case ON conditions for DTL NAND/NOR stage.

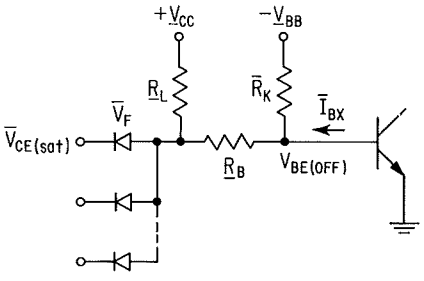


Fig. 10-42. Worst-case OFF conditions for DTL NAND/NOR stage.

The worst-case OFF condition for the above logic circuit is shown in Fig. 10-42; the maximum value of R_K can be expressed

$$\bar{R}_K = \frac{\underline{V}_{BB} - V_{BE(\text{OFF})}}{(\bar{V}_F + \bar{V}_{CE(\text{sat})} + V_{BE(\text{OFF})})/\underline{R}_B + \bar{I}_{BX}} \tag{10-34}$$

Instead of using the R_B resistor to increase OFF-state noise margin of the DTL NAND/NOR gate, one or more diodes may be used to accomplish this purpose.[9] Figure 10-43 shows a circuit in which R_B of Fig. 10-40 has been replaced by two series diodes. In order for Q_1 to be turned on, the voltage level at point A must now rise *above* the sum of the forward-conducting voltages of diodes D_1, D_2, and the base-emitter diode of Q_1.

A worst-case equivalent circuit for the ON condition of the above NAND/NOR stage is shown in Fig. 10-44. This latter circuit is derived from the worst-case circuit of Fig. 10-41, with resistor R_B replaced by the two series diodes. An expression for the minimum value of R_K is now determined to be

$$\underline{R}_K = \frac{\bar{V}_{BB} + \bar{V}_{BE(\text{ON})}}{\dfrac{\underline{V}_{CC} - \bar{R}_L M[\bar{I}_{CEX} + (N-1)\bar{I}_L] - \bar{V}_{BE(\text{ON})} - 2\bar{V}_F}{\bar{R}_L} - \dfrac{N}{\underline{h}_{FE}}\left[\dfrac{\bar{V}_{CC} - \underline{V}_{CE(\text{sat})} - \underline{V}_F}{\underline{R}_L} + (M-1)\bar{I}_L - \underline{I}_2\right]} \tag{10-35}$$

Current I_2 in the above expression is generally less than 0.1 ma and can be neglected to give a more conservative value for R_K.

Figure 10-45 is used to determine a maximum value for R_K. When one input transistor to Q_1 is in saturation, the base voltage of Q_1 must be at the $V_{BE(\text{OFF})}$ level. The voltage at point A is equal to $\bar{V}_{CE(\text{sat})} + \bar{V}_F$, or approximately 1.0 volt for a typical circuit implemented with silicon diodes and low-saturation-voltage

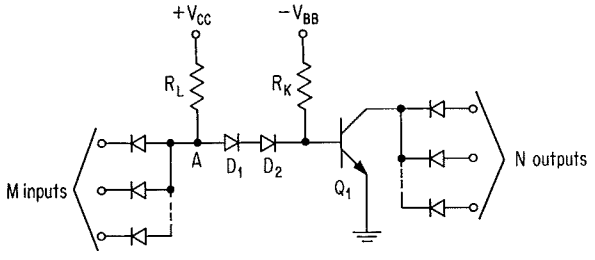


Fig. 10-43. DTL NAND/NOR gate incorporating series diodes to provide noise immunity.

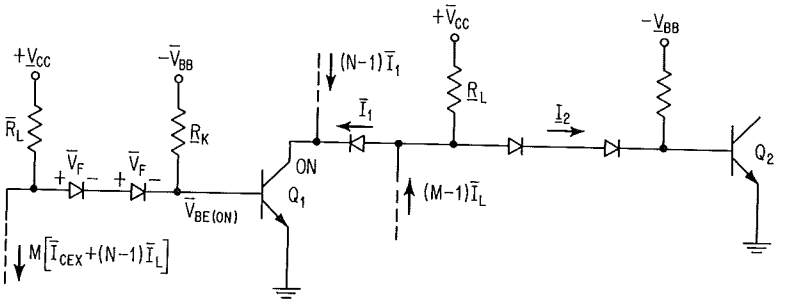


Fig. 10-44. Equivalent circuit depicting worst-case ON conditions for DTL gate of the type shown in Fig. 10-43.

transistors. In order for base voltage of Q_1 to be negative, the voltage drop caused by I_3 flowing through D_1 and D_2 must be larger in magnitude than the positive voltage at point A. The voltage drop across two series-connected silicon diodes is approximately 1.4 volts when these diodes are conducting 50 μa of current. Thus, if D_1 and D_2 are forced to conduct 50 μa of current when Q_1 is at cutoff, the base voltage of Q_1 will be at the level $\bar{V}_{CE(\text{sat})} + \bar{V}_F - 1.4$, or approximately -0.4 volt. It is clear that the actual value of base voltage is dependent upon characteristics of the transistors and the diodes. Current flowing from point B into the $-V_{BB}$ supply consists of $\bar{I}_3$ and $\bar{I}_{BX}$. The maximum value of R_K is given by

$$\bar{R}_K = \frac{V_{BB} - V_{BE(\text{OFF})}}{\bar{I}_3 + \bar{I}_{BX}} \tag{10-36}$$

Integrated-circuit DTL NAND/NOR gates generally utilize diodes in place of R_K as described above. In general, it is difficult to fabricate diffused resistors having tolerances of less than ± 10 per cent. Diodes, on the other hand, may be formed by using the base-emitter or collector-base junction of a transistor. Hence, if the inverter transistor has suitable characteristics, a high yield can be expected for the various diodes within the integrated-circuit chip.

If diodes D_1 and D_2 in Fig. 10-43 are of the slow-recovery type, a transient reverse current flows through the diodes during turnoff; base charge is quickly removed from the inverter transistor, and the circuit turns off rapidly. Discrete diodes such as the 1N645 provide the desired reverse transient current. Slow-

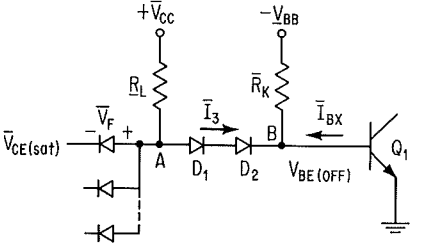


Fig. 10-45. Worst-case OFF conditions for DTL gate of the type shown in Fig. 10-43.

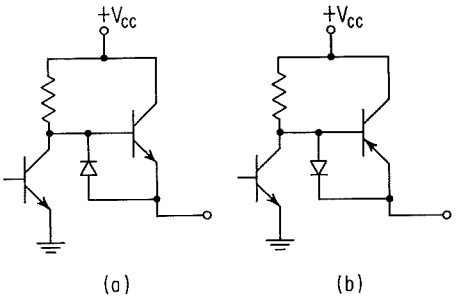


Fig. 10-46. Use of emitter-followers to increase fan-out. *(a)* **N-P-N emitter-follower configuration for TRL and DTL NOR/NAND stages;** *(b)* **P-N-P emitter-follower configuration for DTL NAND/NOR stage.**

recovery diodes are not easily obtained in integrated-circuit form, however, as the gold doping used to reduce minority-carrier lifetime in the transistors also shortens recovery time of the diodes.

10-8. USE OF EMITTER-FOLLOWER TO INCREASE FAN-OUT

The previous two sections have described TRL and DTL circuits in which the collector terminal of a single stage fans out to one or more identical stages. Fan-out capability of a stage was seen to depend upon the amount of current which a stage can source (for the NOR/NAND configuration of TRL and DTL) or upon the amount of current which a stage can sink (for the NAND/NOR DTL configuration).

Fan-out loading of the above logic circuits can be increased by use of emitter-follower transistors connected as shown in Fig. 10-46*a* and *b* (see Sec. 8-5 for a detailed description of these two circuits). The N-P-N emitter-follower serves as a current source to fan-out stages, and the P-N-P emitter-follower serves as a current sink from fan-out stages. Diodes connected from base to emitter of the above emitter-follower transistors serve to discharge any load capacitance. The complementary emitter-follower stage may also be used to increase fan-out loading of an inverter transistor.

When using an emitter-follower stage in the above application, the V_{BE} drop of the emitter-follower transistor must be considered in the design analysis.

10-9. TRANSISTOR-COUPLED LOGIC

One of the more recent developments in transistor logic circuits is shown in Fig. 10-47.[10,*] This logic circuit, which utilizes a multiple-emitter transistor as the coupling element between stages, is variously referred to as a "transistor-coupled logic (TCL) circuit," a "transistor-transistor logic (TTL) circuit," or a "transistor-squared logic (T^2L) circuit." The TCL designation will be used in the present discussion. Because of the requirement for a multiple-emitter transistor, this form of logic circuit is generally available only in integrated-circuit form. For this reason, design of the circuit is done primarily by the semiconductor manufacturer. It is well, however, for the user to understand the design analysis so that

* The number of input emitters may vary from one to approximately eight.

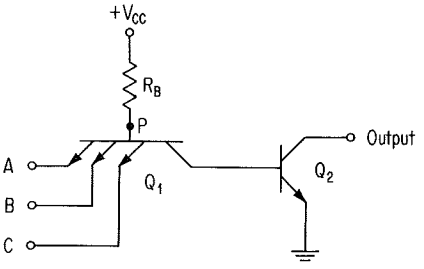


Fig. 10-47. Multiple-emitter coupling transistor provides TCL.

a useful comparison can be made between TCL and the various other forms of logic circuits.

Consider, for the moment, that an input signal is applied only to emitter A in the circuit of Fig. 10-47; no connections are made to emitters B and C. When the input signal is at ground potential, current from the V_{CC} supply flows through R_B, into the base terminal of Q_1, and out of emitter A. The voltage level at point P is equal to the $V_{BE(ON)}$ level of Q_1, or approximately 0.7 volt for a silicon transistor. There is no forward base current to transistor Q_2, as the voltage level at point P is not sufficiently positive to forward-bias both the base-collector diode of Q_1 and the base-emitter diode of Q_2.

Let the input signal level at emitter A now become increasingly positive. The voltage level at point P eventually becomes sufficiently positive for a portion of the base-input current of Q_1 to flow through the base-collector junction of Q_1 and into the base of Q_2. When the voltage level at terminal A rises above the two diode drops seen to the right of point P, the entire current through R_B is steered through the collector of Q_1 and into the base of Q_2; forward base current to Q_2 is now sufficiently large to saturate this device.

If either input terminal in the above figure is now connected to a zero-level input signal, current from point P will flow through a base-emitter diode of Q_1 and into circuit ground. Because of transistor action, forward current flow in an emitter of Q_1 allows *collector* current to flow *into* this device. Initially, collector current of Q_1 is supplied by charge stored in the base of Q_2. Steady-state collector current of Q_1 is simply the collector-base reverse-leakage current of Q_2.

The multiple-emitter transistor performs a logic function which is identical to that of the diode AND/OR gate. Figure 10-48*a* shows the multiple-emitter gate, and Fig. 10-48*b* shows the logically equivalent diode gate. The similarity between the two gate circuits goes beyond the logic equivalence, as the multiple-emitter

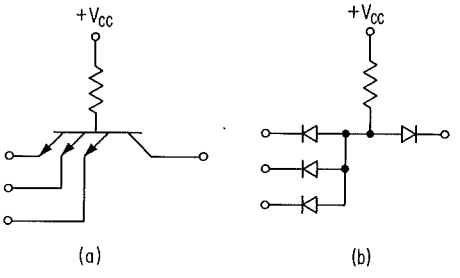


Fig. 10-48. *(a)* **Multiple-emitter transistor;** *(b)* **logically equivalent multi-input diode gate.**

transistor is composed of back-to-back diodes connected in exactly the same manner as the diode gate. However, the important difference between the two gates is that the multiple-emitter transistor exhibits transistor action, whereas the diode gate does not. Transistor action of the multiple-emitter transistor was seen to remove stored base charge in the inverter transistor Q_2 of Fig. 10-47. This rapid removal of base charge permits the TCL circuit to operate at higher speeds than any other logic-circuit configuration utilizing saturated transistors. In addition to the increase in circuit speed, the multiple-emitter transistor provides a path for collector-base reverse-leakage current of the inverter stage. This is in contrast to the diode-gate circuit, which requires a reverse-bias supply voltage to provide a path for transistor leakage current. Because of the logic equivalence between the multiple-emitter transistor and the diode AND/OR gate, the TCL circuit of Fig. 10-47 is designated a NAND/NOR gate.

OFF-state noise margin of the TCL stage is generally in the neighborhood of 0.4 volt at room temperature and often does not exist at elevated temperatures. Consider the circuit of Fig. 10-49, in which transistor Q_1 is turned on and transistor Q_3 is at cutoff.* At room temperature ($+25°C$), and for typical values of circuit components, the voltage level at point A is 0.1 volt, and the saturated-voltage drop of transistor Q_2 is 0.15 volt. This gives a voltage level of 0.25 volt at point B. As approximately 0.65 volt of base-emitter potential is required to turn on Q_3 at least partially at the $+25°C$ temperature, the above circuit has an OFF-state noise margin of 0.4 volt. At an ambient temperature of $+125°C$, saturated-voltage drops of Q_1 and Q_2 may be as large as 0.15 and 0.25 volt, respectively. Because of the high temperature, the base-input voltage of 0.4 volt to Q_3 will allow some forward base current to flow in this device. The above circuit is seen to have zero noise margin at $+125°C$. In actual practice, the situation may not be quite so severe as described above, although OFF-state noise margin of the TCL circuit is extremely small at $+125°C$.

Because of low OFF-state noise margin, the TCL circuit described above has not been widely used. However, a modified form of the basic TCL circuit, which has a suitable OFF-state noise margin, is extensively employed as a logic circuit. This modified, or high-level, form of TCL is described in Sec. 10-10. In order to illustrate circuit features of the high-level TCL, the discussion of the basic TCL continues below.

Two aspects of TCL operation cause current to flow into the emitter of a multiple-emitter transistor.[11] This emitter current has a detrimental effect upon circuit operation. Consider the TCL circuit of Fig. 10-50; emitter A is at a positive level, and base-collector current of Q_1 flows into the base of Q_2. Transistor Q_1 is now operated in the *inverted* mode, with the physical collector of the device serving as an emitter region; a positive voltage level is applied to the physical emitter, and this terminal now acts as a collector region. Current flow into the emitter of Q_1 is dependent upon magnitudes of base current I_B and inverse current gain β_I of the device. This emitter current I_{E1} can be expressed

$$I_{E1} = \beta_I I_B \tag{10-37}$$

and is referred to as "inverse beta current."

* All transistors in Fig. 10-49 are silicon devices.

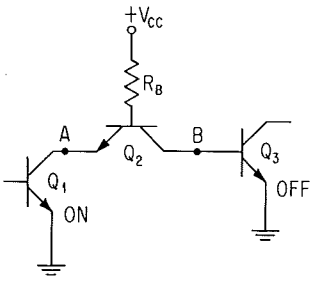


Fig. 10-49. Circuit for consideration of OFF-state noise margin.

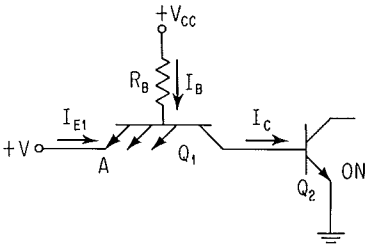


Fig. 10-50. Transistor Q_1 operates in inverted configuration when transistor Q_2 is on.

Figure 10-51 shows a connection of TCL circuits in which transistor Q_1 drives N fan-out transistors. Consider that transistor Q_3 has a somewhat larger base-emitter turn-on voltage drop than that of the other fan-out inverters. For Q_1 at cutoff, fan-out stages Q_4 and Q_6 each require an emitter current given by Eq. (10-37). If voltage at point A is sufficiently low, the current $(N-1)I_{E1}$ will be supplied by current flowing *out* of the emitter of transistor Q_2; this reduces forward base drive to Q_3, as shown in the figure. Fan-out from a stage is limited by magnitudes of I_{E1}, I_B, and the minimum base-current requirement of any inverter transistor. Reduction of R_B will increase the value of I_B, but this increases collector loading of an inverter and hence the minimum required base current. In addition, an increase of I_B increases emitter leakage current I_{E1}.

The second instance of emitter reverse-current flow occurs when a positive-voltage level is applied to an emitter while at least one other emitter of the same multiple-emitter transistor is at ground potential. This circuit configuration is shown in Fig. 10-52*a*; emitter A is at a positive-voltage level, and the remaining emitters are at ground potential. Figure 10-52*b* shows an equivalent circuit for

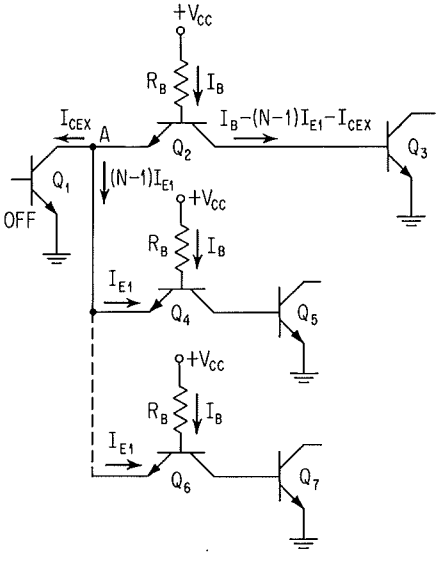


Fig. 10-51. TCL connection in which Q_3 has highest level of $V_{BE(ON)}$ and consequently reduced base drive.

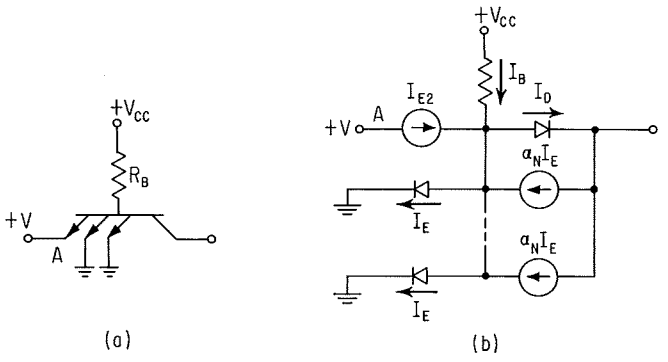


Fig. 10-52. *(a)* **Circuit condition for emitter reverse-current flow;** *(b)* **equivalent circuit.**

this operating condition of the multiple-emitter device.[11] Current I_{E2} into emitter A can be described by

$$I_{E2} = \frac{\alpha_I \alpha_N I_B}{1 - \alpha_I \alpha_N} \tag{10-38}$$

This emitter current, referred to as "input leakage current," is independent of the number of grounded emitters. Typical values of α_I, α_N, and β_N cause I_{E2} to be approximately equal to I_{E1} determined from Eq. (10-37).

Input leakage current is of concern when circuit conditions are as shown in Fig. 10-53. At least one emitter of fan-out transistors Q_4 and Q_6 is at a $V_{CE(\text{sat})}$ potential; base current to transistor Q_3 is reduced by the *total* amount of input leakage current and by the amount of collector reverse-leakage current.

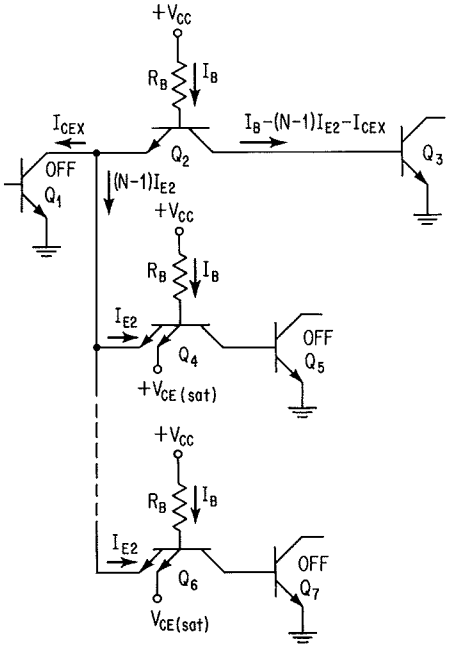


Fig. 10-53. TCL operating condition in which input leakage current I_{E2} reduces forward base drive to Q_3.

Both inverse beta current and input leakage current reduce base drive to an inverter stage by approximately the same amount. These emitter reverse currents can be supplied through a resistor connected from the collector of the output inverter to the V_{CC} supply; this provides increased base drive to the fan-out inverters. However, collector current of a conducting inverter is increased by the addition of the above resistor, and additional base current is required to saturate the inverter.

10-10. HIGH-LEVEL TRANSISTOR-COUPLED LOGIC

Although the TCL circuits described in the foregoing section were shown to be capable of high-speed operation, the OFF-state noise margin was seen to be inadequate for operation at elevated temperatures. An improvement in OFF-state noise margin can be obtained by placing a diode between the multiple-emitter coupling transistor and the input of the inverter transistor; this circuit configuration is shown in Fig. 10-54. The voltage level at point P must now rise above *three* diode drops in order to turn Q_2 on fully. Resistor R_2 provides a discharge path for stored base charge and collector-base leakage current of Q_2.

One disadvantage of the above circuit is that forward base current to Q_2 has a lower maximum value than if diode D_1 were not present. This can be corrected by using the base-emitter diode of a transistor in place of D_1 and utilizing current gain of the added transistor to supply the necessary base current to the inverter transistor. Figure 10-55 shows this latter circuit. Resistor R_3 is selected to provide the desired level of base current to transistor Q_3.

In the circuit of Fig. 10-55, collector and emitter voltage levels of transistor Q_2 have opposite relative polarities. Voltage swing at the collector of Q_2 can be used to drive an additional transistor connected as shown in Fig. 10-56. When Q_2 is turned on, voltage at point A is equal to the sum of base-emitter voltage drop of Q_3 and collector-emitter saturation voltage of Q_2. This can be expressed

$$V_A = V_{BE(\text{ON})} + V_{CE(\text{sat})} \tag{10-39}$$

Transistor Q_3 is turned on when Q_2 is in saturation. Voltage at point B is equal to

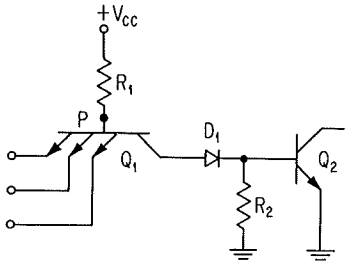


Fig. 10-54. Addition of diode between collector of Q_1 and base of Q_2 to increase OFF-state noise margin of TCL circuit.

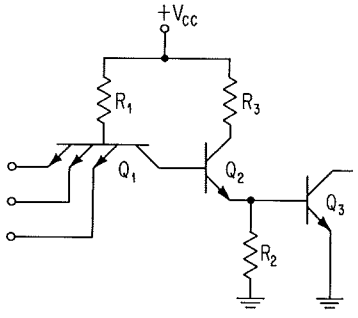


Fig. 10-55. Addition of transistor Q_2 to TCL stage improves OFF-state noise margin of circuit and provides increased base drive to output transistor.

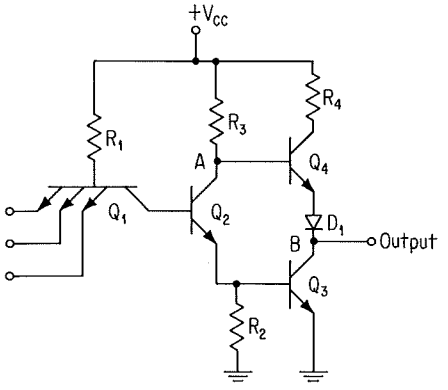


Fig. 10-56. High-level TCL circuit incorporating adequate noise margin with positive drive for both leading and trailing edges of output-voltage waveform.

collector-emitter saturation voltage of Q_3; this voltage can be described by

$$V_B = V_{CE(\text{sat})} \tag{10-40}$$

Equation (10-40) can be subtracted from Eq. (10-39) to give

$$V_A - V_B \approx V_{BE(\text{ON})} \tag{10-41}$$

The above expression is an approximation because the $V_{CE(\text{sat})}$ levels of Q_2 and Q_3 are not necessarily equal. Transistor Q_4 can turn on only if $V_A - V_B$ is larger than the sum of base-emitter forward voltage of Q_4 plus forward-voltage drop V_F of diode D_1. Hence, Q_4 is turned on only if

$$V_A - V_B \geqslant V_{BE(\text{ON})} + V_F \tag{10-42}$$

As Eq. (10-41) shows that the above inequality does not exist when Q_2 is in saturation, Q_4 is off when Q_2 is on. However, when Q_2 turns off, voltage level at point A rises, and transistor Q_4 turns on; transistor Q_3 turns off because there is no forward base current to this device.

Transistors Q_4 and Q_3, together with diode D_1, are connected in a "totem-pole" configuration to provide a positive driving action for both high and low levels of output voltage. When Q_3 is in saturation, circuit output voltage is low, and Q_3 serves as a sink for external current. For Q_3 at cutoff, Q_4 is in conduction and is a source for external current; output voltage rises to a relatively positive level. Transistor Q_4 is seen to be connected in the emitter-follower configuration. Resistor R_4 limits collector current of Q_4.

The above circuit is a modified form of the basic transistor-coupled logic circuit; it is referred to here as a "high-level transistor-coupled logic (high-level TCL) circuit."

In the high-level TCL circuit of Fig. 10-56, the multiple-emitter transistor is not connected to Q_3 and consequently is unable to "pull" this transistor out of saturation. Transistor Q_3 is forced out of saturation, however, by current flow through Q_4. When Q_2 switches from saturation to cutoff, Q_4 turns on before Q_3 turns off. Because both transistors are simultaneously in conduction, a large surge of current flows from the V_{CC} supply into the collector of Q_3; this increased collector current removes minority carriers from the base of Q_3, and the device turns off quickly.

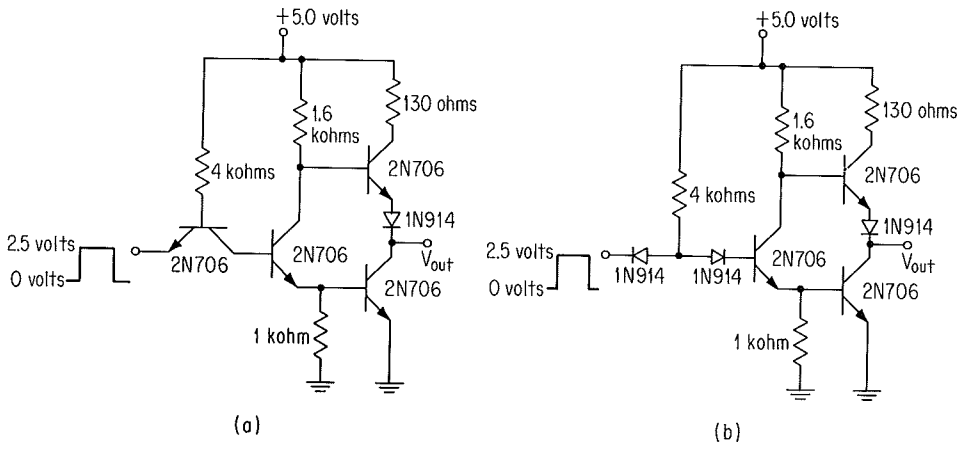


Fig. 10-57. Circuits for comparison of switching speeds. *(a)* **High-level TCL;** *(b)* **same with diodes substituted for coupling transistor.**

The multiple-emitter transistor is effective in turning off Q_2 in the circuit of Fig. 10-56. For this reason, the multiple-emitter input transistor is preferable to a diode-gate input circuit. The above statement is verified by measuring switching speeds of the circuits shown in Fig. 10-57*a* and *b*. These two circuits are identical except for the input portions. Table 10-2 shows measured switching speeds for breadboard models of the two circuits. It is seen that the faster switching speed is obtained with the multiple-emitter transistor gate.

The two emitter reverse currents described for the simple TCL circuit also exist in the high-level TCL circuit. However, in the high-level TCL stage, base current of the multiple-emitter transistor is considerably *larger* when an emitter is grounded than when all emitters are at a positive level; input leakage current is now *larger* than inverse beta current. Thus, only input leakage current is of concern in the high-level TCL circuit.

Circuit Specifications. The high-level TCL circuit shown in Fig. 10-56 is one of the several forms of logic networks which is presently available in integrated-circuit form. Integrated-circuit logic modules eliminate much of the work associated with the design of logic circuits. In addition, use of integrated circuits often reduces the total cost of a system, as much of the hand labor associated with

Table 10-2. Comparison of Switching Times in Nanoseconds for Circuits in Fig. 10-57*

Parameter	Transistor input (Fig. 10-57*a*)	Diode input (Fig. 10-57*b*)
t_d	10	12
t_r	8	15
t_s	20	140
t_f	45	800

* Switching-time intervals are as defined in Fig. 4-10.

assembling components into circuits is eliminated. For these two reasons, many present-day computer and control systems utilize large numbers of integrated-circuit logic modules.

This trend toward use of logic "blocks" focuses attention upon input and output characteristics of the module, with less consideration given to components utilized within the module. The purpose of circuit design is to provide certain desired input and output circuit characteristics. The integrated-circuit logic module is tested for these characteristics by the semiconductor manufacturer. The design engineer is now able to concentrate more upon the complete system, with more of his attention given to logic organization, placement of parts, selection of wiring paths, and the design of interface circuits between various integrated-circuit logic blocks.

Table 10-3 presents typical electrical characteristics of an integrated-circuit version of the high-level TCL stage over a temperature range of -55 to $+125°C$.* These characteristics illustrate one manner in which fan-out and noise margin of a logic network can be specified. In addition, the circuit is shown to operate satisfactorily for a shorted output. Positive logic is used in the table. The logic stage is designed to operate over a supply-voltage range of 4.5 to 5.5 volts.

An explanation of the various data-sheet parameters is given below. In order to describe the various tests, it is necessary to refer to various configurations of the high-level TCL circuit. Instead of showing the complete schematic diagram of the circuit, a logic diagram of a NAND/NOR gate is used. This diagram is shown in Fig. 10-58. The large portion of the diagram represents an AND/OR

* These electrical characteristics correspond closely to data-sheet values for the SN5400 integrated circuit manufactured by Texas Instruments Incorporated.

Table 10-3. Electrical Characteristics of High-level TCL Circuit at $T = -55$ to $+125°C$

Test	Parameter	Test conditions	Min	Max	Unit
1	$V_{in(1)}$ logical 1 input voltage	$V_{CC} = 4.5$ volts $V_{out} \leqslant 0.4$ volt $I_{load(sink)} = 16$ ma	2.0	...	volts
2	$V_{out(0)}$ logical output voltage	$V_{CC} = 4.5$ volts $V_{in} = 2.0$ volts $I_{load(sink)} = 16$ ma	...	0.4	volts
3	$V_{in(0)}$ logical 0 input voltage	$V_{CC} = 4.5$ volts $V_{out} \geqslant 2.4$ volts $I_{load(source)} = 0.4$ ma	...	0.8	volts
4	$V_{out(1)}$ logical 1 output voltage	$V_{CC} = 4.5$ volts $V_{in} = 0.8$ volt $I_{load(source)} = 0.4$ ma	2.4	...	volts
5	I_{in} input current	$V_{CC} = 5.5$ volts $V_{in} = 0.4$ volt	...	1.6	ma
6	I_L input leakage current	$V_{CC} = 5.5$ volts $V_{in} = 4.5$ volts	...	40	μa
7	I_{short} short circuit output current	$V_{CC} = 5.5$ volts	...	55	ma

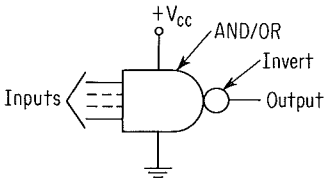


Fig. 10-58. Logic-block representation of NAND/NOR gate.

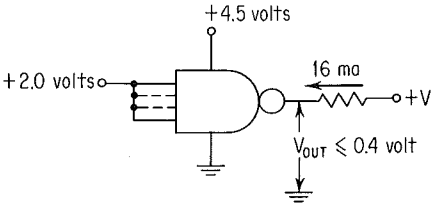


Fig. 10-59. Circuit conditions for tests 1 and 2.

gate and shows the number of input terminals. The inverter portion of the NAND/NOR gate is represented by a circle.

Tests 1 and 2. Refer to Fig. 10-59. A logical 1 for V_{in} gives a logical 0 for V_{out}. The voltage level of 2.0 volts to each input is sufficiently positive to saturate the output inverter. Output voltage of the stage is at a maximum level of 0.4 volt for 16 ma of current flow *into* the stage.

Power-supply voltage for the first four tests is given as 4.5 volts. This minimum value of V_{CC} is a worst-case supply voltage for these four tests.

Tests 3 and 4. Refer to Fig. 10-60. Each input emitter is alternately connected to 0.8 volt, with all other emitters connected to 4.5 volts. The 0.8-volt level is sufficiently low to maintain circuit output voltage at a positive level of 2.4 volts or greater. A load current of 0.4 ma flows *out* of the stage for these tests.

Test 5. Refer to Fig. 10-61. Each input emitter is alternately connected to 0.4 volt; all other emitters are connected to 4.5 volts. This test is a measure of total emitter current under worst-case loading conditions. A maximum emitter current of 1.6 ma is specified.

Power-supply voltage for this test, and for the following two tests, is given as 5.5 volts. This voltage is a worst-case level of V_{CC} for these tests.

Test 6. Refer to Fig. 10-62. Each input emitter is alternately connected to 4.5 volts; all other emitters are grounded. The leakage current *into* an emitter has a maximum value of 40 μa.

Test 7. Refer to Fig. 10-63. All input emitters are grounded; the output terminal is grounded, and a maximum current of 55 ma is specified.

Fan-out. Test 5 shows that for an input level of 0.4 volt, current into the 0.4-volt source will not exceed 1.6 ma. If 10 stages are driven from a single stage of the type under discussion, not more than 16 ma will flow *into* the output

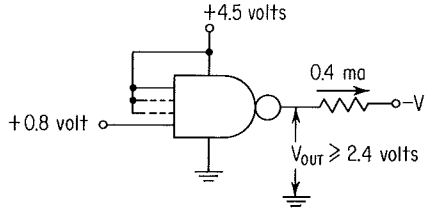


Fig. 10-60. Circuit conditions for tests 3 and 4; each input tested separately.

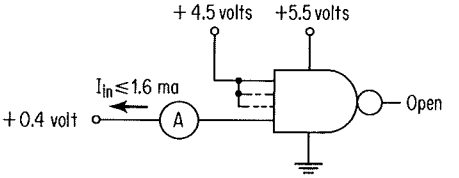


Fig. 10-61. Circuit conditions for test 5; each input tested separately.

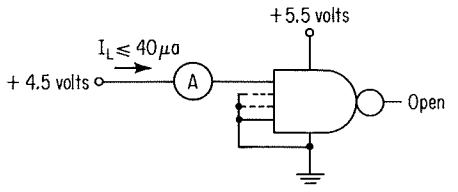


Fig. 10-62. Circuit conditions for test 6; each input tested separately.

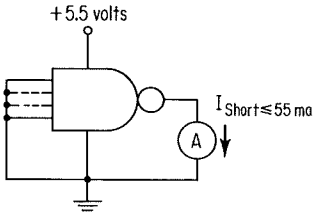


Fig. 10-63. Circuit conditions for test 7.

terminal of the driver stage when this terminal is at a potential of 0.4 volt. This 16-ma current level is the load current for tests 1 and 2. These latter two tests show that an input of 2.0 volts is sufficient to maintain 0.4 volt maximum of output voltage for a load current of 16 ma into the inverter. Hence, the circuit can *absorb* the current from 10 fan-out stages.

From test 6, input leakage current to a stage is not greater than 40 μa. This shows that a single stage must source a maximum total current of 0.4 ma to 10 fan-out loads. Tests 3 and 4 indicate that the circuit can source 0.4 ma of load current and maintain an up-level output voltage of 2.4 volts or greater.

The above considerations show that the circuit has a minimum fan-out of 10.

Noise Margin. ON- and OFF-state noise margins are determined from tests 1 to 4. Tests 1 and 2 show that an input voltage as low as 2.0 volts will maintain the output terminal at a voltage not greater than 0.4 volt for a load of 16 ma into the output terminal. Tests 3 and 4 show that an input signal as large as 0.8 volt will maintain the output terminal at a voltage greater than or equal to 2.4 volts for a 0.4-ma current flow out of the output terminal.

In tests 1 and 2, the circuit is tested at a minimum input voltage of 2.0 volts for an output voltage not greater than 0.4 volt. However, tests 3 and 4 are performed with an input signal of 0.8 volt, and the output voltage is not less than 2.4 volts. In order to turn the circuit on, only 2.0 volts is required, whereas a minimum of 2.4 volts is available from an OFF stage. This gives the circuit an ON-state noise margin of 0.4 volt. Also, although 0.8 volt is sufficiently low to turn off a stage, the down-level output voltage from an ON stage is not greater than 0.4 volt. OFF-state noise margin is thus seen to have a value of 0.4 volt. These noise margins are minimum values for a fan-out loading of 10 over the temperature range of -55 to $+125°C$.

10-11. WIRED LOGIC

Output signals from logic circuits can often be combined directly to obtain useful logic functions. An example of this is illustrated by the circuit diagram of Fig. 10-64. Each inverter stage provides an output signal which is the complement of its input signal. However, as the two collectors are wired together, the circuit output signal is given by

$$\text{Output} = \bar{A}\bar{B} \tag{10-43}$$

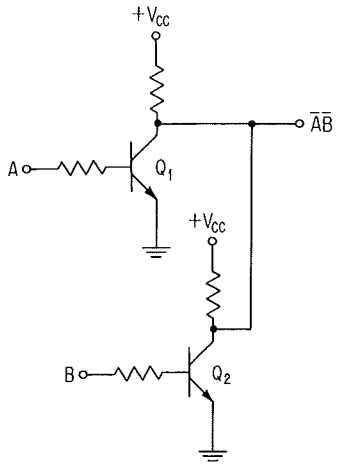


Fig. 10-64. Wired-AND circuit configuration.

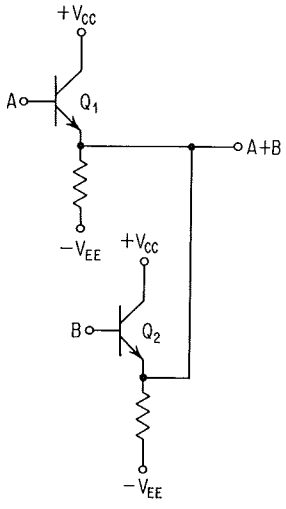


Fig. 10-65. Wired-OR circuit configuration.

for positive logic. This form of logic connection is referred to as a "wired-AND configuration."

Only one collector load resistor is required in the above circuit. The collectors of additional transistors can be connected at the output terminal to extend the AND expression of Eq. (10-43).

Wired-OR logic can be performed by connecting the emitters of two or more emitter-follower transistors. This technique is shown in Fig. 10-65 for two emitter-follower stages. For positive logic, the output of this circuit can be expressed

$$\text{Output} = A + B \tag{10-44}$$

A single emitter-resistor can be used in the above circuit. The OR combination of additional variables is implemented by increasing the number of emitter-follower devices.

Except for the high-level transistor-coupled logic circuit, all other logic circuits described in this chapter can be wired together at their output terminals to obtain an additional stage of logic. When this is done, the load resistor should be that associated with a single stage; otherwise, the various load resistors are in parallel with each other and may cause excessive loading when only one logic circuit is conducting current.

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11

Current-mode Switching Circuits

11-1. NONSATURATED VERSUS SATURATED SWITCHES

It was pointed out in Sec. 1-4 that a transistor is considered to be in saturation when the device is biased to operate in region III. In this state of operation, the forward-biased emitter injects more carriers into the base region than the collector is able to remove; the collector-base junction is no longer reverse-biased. If this junction is sufficiently forward-biased, the collector region injects additional carriers into the base.

From the foregoing discussion, transistor saturation is defined to be the operating condition for which base charge is in excess of that required to maintain the maximum allowable collector current.[1] Conversely, a nonsaturated transistor is one in which no excess charge is allowed to accumulate in the base region; this is accomplished by designing the switching circuit so that transistor operation does not enter region III.

Although charge-storage effects do not exist in the nonsaturated transistor, the device experiences an increased power dissipation over that associated with saturated operation. This is the result of a relatively large collector-emitter voltage drop in the nonsaturated device, as contrasted to the $V_{CE(\text{sat})}$ level of a saturated transistor.

11-2. PREVENTING SATURATION OF INVERTERS

Figure 11-1 shows a circuit which utilizes a "collector-catcher" diode to prevent transistor saturation.[1] The action of this diode is similar to that of the plate-catching diode employed with vacuum-tube switches.[2] When collector-emitter voltage falls below the level of $V - V_F$ (the diode forward-voltage drop), the diode conducts, and V_{out} is clamped to the $V - V_F$ voltage level. Collector current is not limited by R_L, as the forward-biased diode provides an additional path for current flow to the collector; collector current now rises to the $h_{FE}I_B$ level.

An excessively large power dissipation may occur in the above circuit, especially if the transistor is a high-gain device. The clamped level of collector voltage must

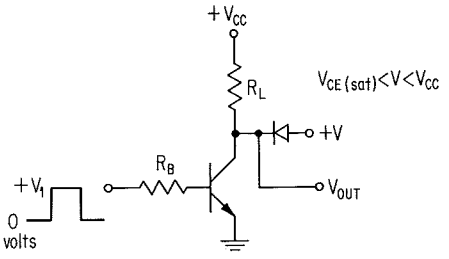

Fig. 11-1. Use of collector-catcher diode to prevent saturation.

be sufficiently positive to keep the transistor out of saturation. This voltage level is given by

$$V_{CE} \geqslant r_{CE(\text{sat})} h_{FE} I_B \tag{11-1}$$

In order to accommodate transistors having a spread of h_{FE} values, the above inequality must be satisfied for the device having the largest value of h_{FE}. This particular transistor will also have the largest collector current and consequently the largest power dissipation of all devices.

Current from the $+V$ supply-voltage source in Fig. 11-1 is relatively large. If several of these circuits are connected to the $+V$ voltage source, the required current-handling capability of this voltage source may become prohibitively high.

Transistor saturation can also be prevented by limiting voltage drop across the collector load resistor to a value small enough to prevent the collector-base junction of the device from becoming forward-biased. The above voltage drop can be maintained within acceptable limits by controlling the magnitude of emitter current. This method of avoiding saturation is incorporated in the current-mode switch described in the following section.

11-3. CURRENT-MODE SWITCH

A basic innovation in the design of nonsaturated switching circuits has been development of the current-mode switch (CMS).[3] This high-speed switching circuit is useful for performing logical operations. The following discussion presents an explanation of the basic CMS. Refined versions of this basic circuit are described later in Secs. 11-5 and 11-6.

Figure 11-2 shows an original form of the CMS. Two transistors and two power supplies are used in the circuit. For purposes of analysis, transistors Q_1 and Q_2 are assumed to be silicon devices. However, circuit operation is similar when the two transistors are germanium devices.

Consider that the circuit of Fig. 11-2 has an input-signal level of $+0.5$ volt. Let us assume that this positive-input level turns on Q_1 (it is shown below that Q_1 is indeed conducting). The base-emitter voltage drop of Q_1 has a nominal magnitude of 0.7 volt, and the voltage at point A is equal to -0.2 volt. The base terminal of Q_2 is at ground potential, and the base-emitter diode of this transistor has a forward-bias voltage of 0.2 volt. However, as approximately 0.5 volt is required to turn on a silicon transistor at least partially, Q_2 is not conducting. Hence, Q_1 is turned on, and current through R_E flows only from the emitter of Q_1. Emitter current of Q_1 is designated I_{E1}.

Collector current of Q_1 is given by the product $\alpha_N I_{E1}$. An expression for collector voltage of Q_1 can be written

$$V_{C1} = V_{CC} - \alpha_N I_{E1} R_{L1} \tag{11-2}$$

Circuit design is such that the term $\alpha_N I_{E1} R_{L1}$ in Eq. (11-2) is equal to approximately 1 volt. Supply voltage V_{CC} is made sufficiently positive for V_{C1} of Eq. (11-2) to be more positive than the +0.5-volt input signal. This assures that the collector of Q_1 cannot become negative with respect to its base; hence, the transistor cannot saturate.

For an input-signal level of −0.5 volt to Q_1, let us assume that Q_2 is turned on. The emitter-base forward-voltage drop of Q_2 causes point A to acquire a nominal voltage level of −0.7 volt. Transistor Q_1 now has −0.5 volt applied to its base and −0.7 volt applied to its emitter. This latter device is forward-biased at its input by only 0.2 volt and consequently is at cutoff. Collector voltage of Q_1 is now given by

$$V'_{C1} = V_{CC} - I_{C(\text{off})} R_{L1} \tag{11-3}$$

where $I_{C(\text{off})}$ is the OFF-state collector current of Q_1.

Current at the common-emitter connection of Q_1 and Q_2 is seen to be switched into the emitter of Q_1 or into the emitter of Q_2. However, the ON-state emitter currents of the two devices are not identical. Emitter current is determined by the voltage drop across R_E and the magnitude of this resistor. Voltage at point A is equal to −0.2 volt when Q_1 is turned on and is equal to −0.7 volt when Q_2 is turned on. Hence, emitter current of Q_1 is larger than that of Q_2. Load resistor R_{L1} is generally selected to be slightly smaller than R_{L2} in order to provide the same voltage swing at the two output terminals.

ON-state emitter current of the two transistors in the above circuit can be made nearly equal by using a large negative voltage for $-V_{EE}$ and a large resistor for R_E. With $-V_{EE}$ many times larger than the total voltage excursion at point A, R_E and $-V_{EE}$ effectively become a constant-current source. Current through R_E is then given by

$$I_E = \frac{V_{EE}}{R_E} \tag{11-4}$$

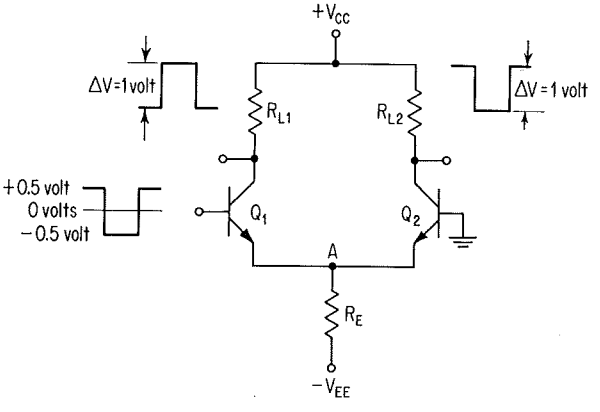

Fig. 11-2. Current-mode switch.

In the CMS of Fig. 11-2, the collector signal of Q_1 is inverted with respect to the circuit input signal; an in-phase component of output voltage is obtained from the collector of Q_2. Transistors can be paralleled at the input of the CMS, as shown in Fig. 11-3, to provide the NOR/NAND function at output $\bar{P}$ and the OR/AND function at output P. Diode AND gates can be used to drive an input transistor of the CMS.[4] Hence, the CMS can be used to provide various combinations of logic functions.

Input- and output-voltage swings of the CMS are nominally equal to 1 volt peak to peak. Because of these small voltage swings, switching thresholds at the input terminal are reached in less time than that associated with most saturated switching circuits.

Collector-base voltage and collector-emitter voltage of a transistor in the CMS are larger than corresponding voltage drops in the saturated transistor. Figure 5-11 shows that C_{ob} decreases with an increase in V_{CB}. Also, from Fig. 5-12, an increase in V_{CE} is seen to increase f_t of the transistor. Transient response of the CMS is aided by the relatively low value of C_{ob} and the relatively high value of f_t.

Effects of load capacitance are reduced in the CMS by using load resistance in the range of 50 to 100 ohms. In order to obtain a voltage swing of 1 volt peak to peak at a collector terminal, ON-state collector current of a device varies from 20 to 10 ma, depending upon the particular value of load resistor. The relatively low values of load resistance and high values of collector currents allow load capacitance to charge and discharge quickly.

Because of the circuit features described above, the CMS is the fastest type of switching circuit. This switching-speed advantage is achieved at the expense of increased power consumption over that of saturated switching circuits. Emitter current flows continuously in the CMS; to a close approximation, average power dissipation P_T of the entire circuit is given by

$$P_T = I_E(V_{EE} + V_{CC}) \tag{11-5}$$

This power dissipation is generally higher than average power dissipation of a saturated switching circuit.

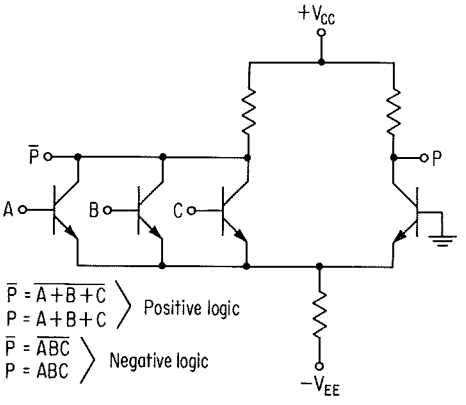

Fig. 11-3. Addition of parallel input transistors to increase logic capability of current-mode switch.

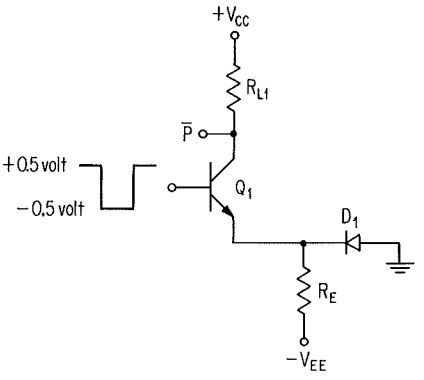

Fig. 11-4. Current-mode switch which provides the complementary output signal only.

Both true and complementary output signals are obtained from the CMS. However, the true output signal is often not required in various logic portions of a system. If this is the case, transistor Q_2 in the circuit of Fig. 11-2 can be replaced by a diode, as shown in Fig. 11-4. Operation of the above two circuits is identical, except that input current to diode D_1 of the latter circuit flows into circuit ground instead of dividing between the base and collector regions of a transistor. In many instances, only the true output signal is required. The collector terminal of Q_1 can then be connected directly to $-V_{CC}$ in Fig. 11-2. This reduces input capacitance to Q_1, and the circuit operates at a slightly higher speed.

Output signals of the CMS in Fig. 11-2 are close to the $+V_{CC}$ level, whereas the input signal varies about ground potential. Thus, the output signal of a CMS cannot be used directly to drive an identical circuit. One method of cascading CMS circuits is to use opposite-polarity transistors in alternate circuits. Figure 11-5 shows a connection of this type. The base of Q_2 is connected to ground potential; this sets the input switching threshold of the N-P-N stage at 0 volts. An input signal of ± 0.5 volt to Q_1 causes an output-voltage swing of approximately 1 volt at the collector of Q_2. Collector supply voltage of the N-P-N circuit is shown as $+6$ volts, and output voltage varies (approximately) from $+6$ to $+5$ volts. The

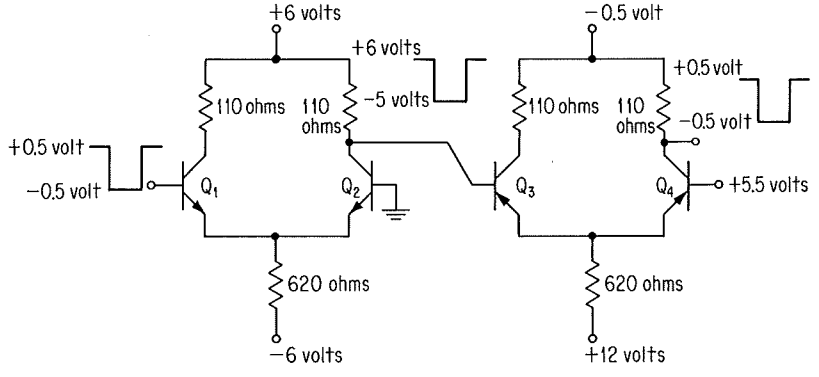

Fig. 11-5. Cascade connection of current-mode switches; opposite-polarity transistors are used in alternate stages.

+5.5-volt level applied to the base of Q_4 sets the input switching threshold of the P-N-P stage at +5.5 volts. Hence, the input signal to Q_3 is at the correct level to cause switching of the P-N-P stage. The output-voltage swing from Q_4 varies about ground potential and is adequate to drive a succeeding N-P-N stage.

Transistors of the same polarity may be used in alternate CMS circuits only if input and output signals vary about the same dc level. A shift of output-voltage level can be accomplished in the circuit of Fig. 11-2 by use of a zener diode and a biasing resistor. However, as a result of advances in the fields of transistor technology and circuit design, certain transistors of the same polarity may be used in alternate stages of carefully designed CMS circuits without requiring any form of voltage translation between stages. Circuits of this latter type are described in Secs. 11-5 and 11-6.

11-4. TRANSISTORS FOR SATURATED HIGH-SPEED OPERATION

Alloy- and grown-junction transistors exhibit an increase in storage time as a result of operation into region III. Collector current of these devices does not diminish significantly until excess charge is removed from the *base* region. Storage effects are also evident in diffused-base transistors, although for a different reason. When the collector-base junction of a diffused-base transistor becomes forward-biased, the base injects carriers into the collector region; because of a relatively high collector resistivity, these carriers are unable to recombine quickly in the collector region. Thus, storage time in the diffused-base structure is the result of minority-carrier storage in the collector region.

The diffused-base epitaxial transistor exhibits only a small amount of collector storage, as pointed out in the discussion of Sec. 3-6. Charge-storage effects are not significant in this type of device until the collector-base junction becomes sufficiently forward-biased for the collector to inject carriers into the base region: this occurs at a voltage level of approximately 0.2 volt for a germanium transistor and approximately 0.5 volt for a silicon device. For this reason, these types can be operated slightly into region III and yet have low storage-time characteristics. Because the junction turn-on voltage is larger for a silicon transistor than for a germanium device, the circuits described below are implemented with diffused-base epitaxial *silicon* transistors.

Certain types of diffused-base epitaxial silicon transistors are found to have good frequency-response characteristics for small forward bias of the collector-base junction.[5] This is a result of the built-in field of the base region, together with a narrow base and a low-resistance collector region. Transistors of this type provide high-speed operation when used in lightly saturated switching circuits; the 2N3832 transistor falls into this category.

11-5. SATURATED CURRENT-MODE SWITCH

The ability of a transistor to operate into saturation without experiencing an excessive storage delay is of use in circuits only to the extent that the degree of saturation can be controlled. The current-mode switch (CMS) described in Sec. 11-3 gives precise control of emitter current and hence of collector-base junc-

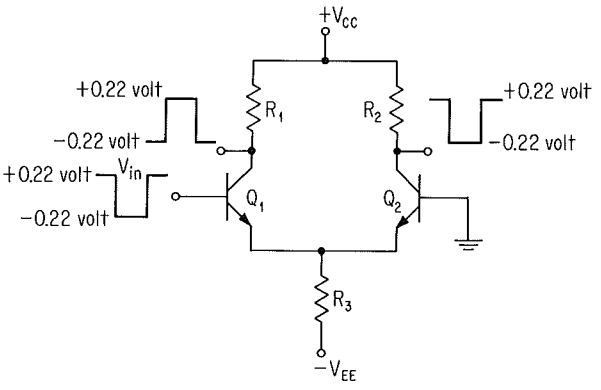

Fig. 11-6. Circuit of saturated current-mode switch.

tion potential. By allowing collector-base diodes in the CMS to become slightly forward-biased, the output of one stage can be coupled *directly* to the input of a succeeding stage.[6] Circuits of this type are referred to here as "saturated current-mode switches." Figure 11-6 shows a schematic diagram of the saturated CMS, together with typical input- and output-voltage levels. The circuit configuration is identical to that of the CMS in Fig. 11-2, although component values are now different. The discussion below will show that the value of V_{CC} used for the circuit of Fig. 11-6 permits the transistors to saturate, whereas the V_{CC} level in Fig. 11-2 was chosen to prevent transistor saturation.

DC Analysis. Because of the small input- and output-voltage swings, together with the nonlinear relationship between current and voltage of a base-emitter diode, operating-current levels of a saturated CMS circuit are best determined by a graphical analysis. Emitter currents are obtained from a graphical analysis of the input portion of the circuit and are then multiplied by common-base dc current gain α_N to obtain collector current. The following analysis applies specifically to the circuit configuration of Fig. 11-6, although the technique is identical for other types of CMS circuits.

Consider the input portion of the circuit in Fig. 11-6. This consists of the input signal V_{in}, two base-emitter diodes, resistor R_3, and supply voltage $-V_{EE}$. These elements are interconnected as shown in the circuit of Fig. 11-7. Diodes D_1 and D_2 represent base-emitter diodes of transistors Q_1 and Q_2, respectively. The figure shows that for $V_{\text{in}} = 0$, current I_{E0} divides equally between the two diodes. As V_{in} increases in a positive direction, I_{E1} becomes larger while I_{E2} diminishes. Conversely, as V_{in} becomes increasingly negative, I_{E2} increases and I_{E1} decreases. By adjusting the level of V_{in}, current through R_E can be made to flow almost entirely through D_1 or D_2. Currents I_{E1} and I_{E2} are determined below for the two extremes of input-voltage swing ($+0.22$ and -0.22 volt).

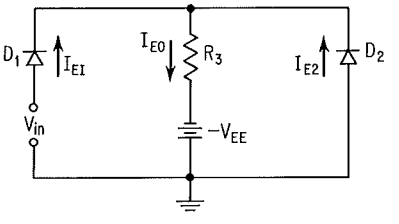

Fig. 11-7. Equivalent input circuit for saturated current-mode switch of Fig. 11-6.

Current I_{E1} is determined first. This current

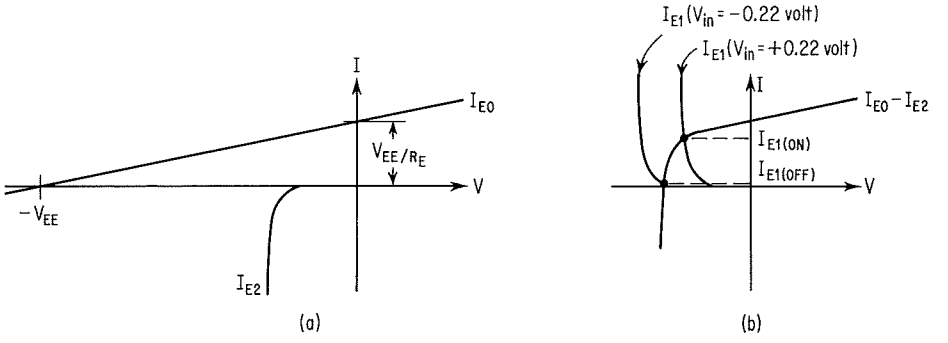

Fig. 11-8. Graphical analysis to determine current through D_1 in circuit of Fig. 11-7. *(a)* **Individual plots of I_{E2} and I_{E0};** *(b)* **composite plot and plots of I_{E1} for two values of V_{in}.**

can be expressed

$$I_{E1} = I_{E0} - I_{E2} \tag{11-6}$$

Figure 11-8*a* shows individual plots of I_{E0} and I_{E2}.* The composite plot obtained by subtracting I_{E2} from I_{E0} is shown in Fig. 11-8*b*, which also shows plots of I_{E1} for $V_{in} = +0.22$ volt and $V_{in} = -0.22$ volt. The intersection of an I_{E1} plot with the composite curve gives I_{E1} for the particular value of V_{in}. It is seen that $I_{E1(ON)}$ is relatively large, while $I_{E1(OFF)}$ is close to zero.

Figure 11-9 illustrates the procedure for obtaining ON and OFF levels of I_{E2}. Figure 11-9*a* shows a plot of I_{E0}, together with plots of I_{E1} for the two extremes of V_{in}. Current I_{E2} can be written

$$I_{E2} = I_{E0} - I_{E1} \tag{11-7}$$

Figure 11-9*b* shows composite plots of $I_{E0} - I_{E1}$ for the two levels of V_{in}. This portion of the figure also shows a plot of I_{E2}. Currents $I_{E2(ON)}$ and $I_{E2(OFF)}$ are determined by the intersections of the I_{E2} plot with the two composite curves. A

* The material of Chap. 8 provides a background for the present analysis.

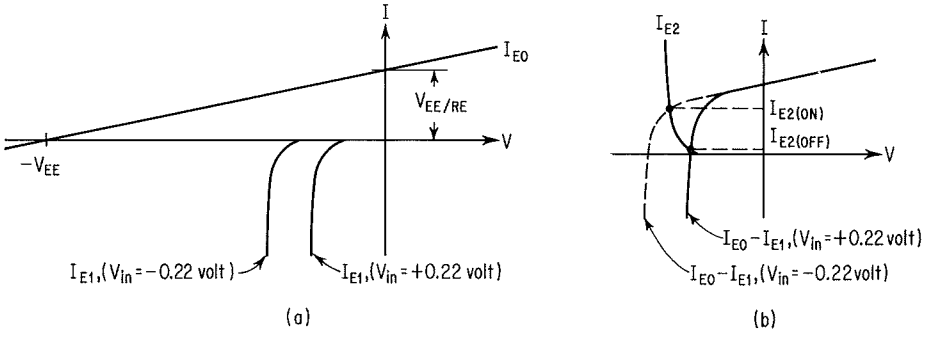

Fig. 11-9. Graphical analysis to determine I_{E2} in Fig. 11-7. *(a)* **Plot of I_{E0} and plots of I_{E1} for two values of V_{in};** *(b)* **composite plots and plot of I_{E2}.**

significant difference is seen to exist between ON and OFF levels of I_{E2}. Also, $I_{E2(ON)}$ is found to be slightly *smaller* than $I_{E1(ON)}$.

This graphical procedure can be extended to include the effects of more than one input transistor. Figure 11-10*a* shows a saturated CMS having three input transistors. Each of these transistors has a different level of input signal. Figure 11-10*b* shows the equivalent input circuit for the above stage; the input-signal levels are included in this latter circuit. The value of any branch current in this equivalent circuit can be determined by forming a composite *VI* plot of all other branch currents. The *VI* plot of the branch under investigation is then superimposed on the composite plot; the intersection of these two plots gives the sought-after current level.

Let us return now to the circuit configuration of Fig. 11-6 and consider the relationship between input- and output-voltage levels. From the preceding graphical analysis, emitter currents can be obtained for various values of input-signal level. These currents are multiplied by α_N of the individual transistors to obtain collector currents. For any state of transistor conduction, output voltage can be described by

$$V_{\text{out}} = V_{CC} - (I'_C + I_L)R_L \tag{11-8}$$

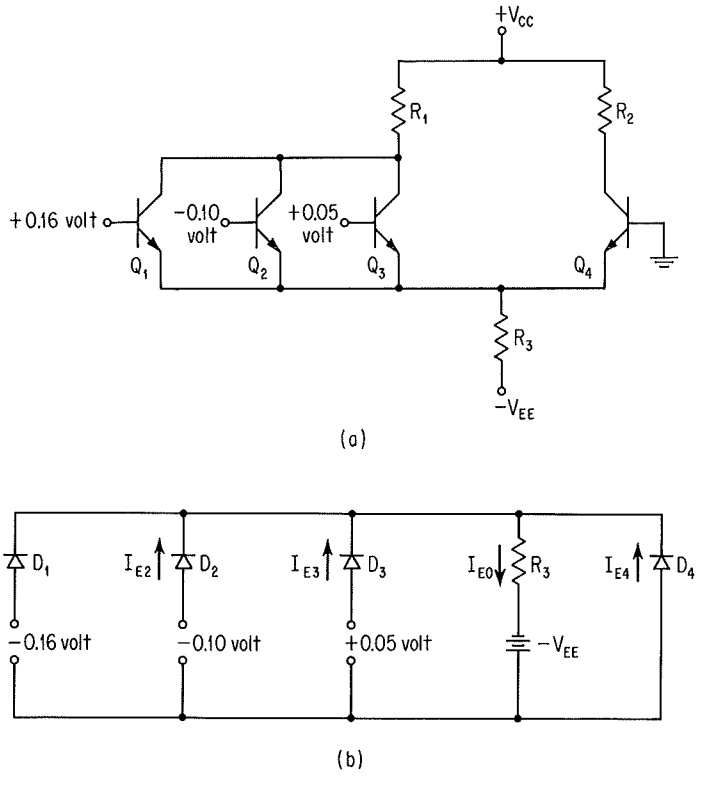

Fig. 11-10. *(a)* **Saturated CMS having three input transistors;** *(b)* **graphical analysis of circuit.**

where V_{out} = output voltage at collector terminal
I'_C = *total* collector current
I_L = current through R_L into external load

When a transistor is at the OFF state, an extremely small emitter current (and hence collector current) flows through the device; in addition, there is a reverse-leakage current through the collector-base junction. These two collector currents, together with any current through R_L into a fan-out load, give an OFF-state collector (output) voltage which is below the level of V_{CC}. A transistor in the ON state has a relatively large collector current; collector voltage is at a negative level, and there is negligible current flow to an external load. Collector-base current of the conducting transistor is also negligible *except* when the transistor saturates. The saturated device has a collector-base current flow which *opposes* the normal flow of collector current; total collector current is reduced, and collector voltage is clamped to one diode drop below the level of base voltage.

Upper and lower limits for output-voltage level are fixed by the allowable magnitude of forward-bias voltage across a collector-base diode. Collector-base voltage of a transistor is given by*

$$V_{CB} = V_{\text{out}} - V_B \tag{11-9}$$

where V_{CB} = voltage at collector measured with respect to base
V_{out} = output voltage at collector terminal, given by Eq. (11-8)
V_B = base voltage measured with respect to ground potential

The V_B term in the above expression is equal to zero for transistor Q_2, as the base terminal of this device is connected to ground potential. Transistor Q_1, however, has a base-input signal which does rise to a positive level. Also, compared to Q_2, transistor Q_1 has a larger collector current and consequently a more negative level of V_{out} when turned on. Transistor Q_1 has the larger forward-bias collector-base voltage of the two devices; hence, Eq. (11-9) will be applied to Q_1.

From Eq. (11-9), the most negative value of V_{CB} occurs when V_{out} is at its *most negative down level* (MNDL) and V_B is at its *most positive up level* (MPUL). The above expression for V_{CB} can now be rewritten

$$V_{CB} = \text{MNDL} - \text{MPUL} \tag{11-10}$$

The output voltage of a stage becomes the input voltage to a succeeding stage. Thus, the two terms on the right side of Eq. (11-10) are out-of-phase components of the same signal voltage. Let these two voltage levels be considered the two extremes of base-voltage swing. For a typical circuit, the required *least positive up level* (LPUL) of base voltage is approximately 0.2 volt. In order to provide this minimum value of positive-signal level, collector-supply voltage V_{CC} has a value of approximately 0.25 volt. Consider that V_{CC} is *exactly* 0.25 volt and that both collector reverse-leakage current and external-load current through R_L are negligibly small. This, then, gives a MPUL of 0.25 volt for the right side of Eq. (11-10). The MNDL term of Eq. (11-10) is determined from a consideration of the *most*

* Because V_{out} and V_B can take on either positive or negative values, the positive or negative sign associated with a voltage level must be used in Eq. (11-9).

negative allowable level of V_{CB}; this V_{CB} level is approximately 0.5 volt for a silicon planar epitaxial transistor (for V_{CB} more negative than approximately 0.5 volt, the collector-base junction becomes sufficiently forward-biased to cause significant storage time). Substitution of 0.25 and 0.5 volt, respectively, for the MPUL and V_{CB} terms of Eq. (11-10) yields a MNDL of -0.25 volt for the base signal of a saturated CMS.

Figure 11-11 shows typical plots of output voltage versus input voltage for the saturated CMS. Curves A and B respectively correspond to the collector-voltage levels of Q_2 and Q_1 in the circuit of Fig. 11-6. Curve A is taken from the noninverting transistor and is the *true* output signal. The inverting transistor gives the *complementary* output signal, as shown by curve B. A point of inflection is evident in the negative portion of curve B. At an input-voltage level corresponding to V', transistor Q_1 saturates, and *total* collector current decreases; output voltage of Q_1 becomes less negative for further increase of V_{in}.

For any system of logic elements, an input signal to one stage is propagated through all succeeding stages. The resulting input signal to each stage must have adequate ON and OFF levels to control the states of that stage properly. Certain types of logic systems incorporate circuit elements which attenuate the signal propagated through them. For instance, voltage swings are reduced by emitter-follower stages and by diode gates; the magnitude of available current is reduced by diode gates and by common-base stages. If the control signal is allowed to diminish continually as it passes through successive stages, it will eventually become too small to be useful. This degradation of control signal can be maintained within acceptable limits by utilizing amplifying elements at various points throughout the system. These amplifiers may simply be transistor inverters, which provide both current gain and voltage gain.

Logic systems incorporating the saturated CMS require no additional amplifying elements. This implies that signal gain of a stage must be at least as large as unity. A small base current controls a much larger collector current in the above circuit. Hence, current gain of a stage is considerably greater than unity. However, care must be taken to assure that *voltage gain* of the circuit is also maintained at or above the unity level.

Component tolerances of the saturated CMS cause output-voltage response to vary from one circuit to the next. Figure 11-12 shows two plots of in-phase output-voltage level versus input-voltage level for the present circuit. These curves, labeled 1 and 2, are the result of extreme variations for circuit parameters.

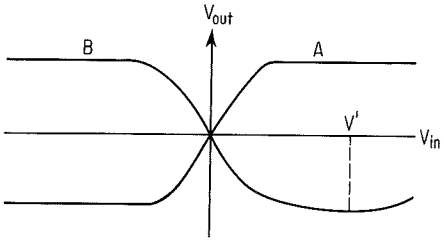

Fig. 11-11. Typical plots of V_{out} versus V_{in} for saturated CMS.

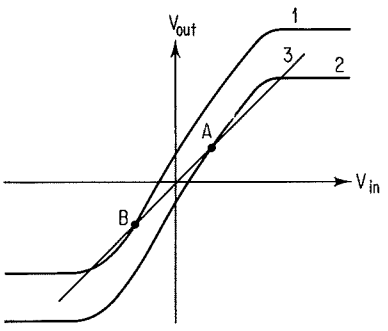

Fig. 11-12. In-phase V_{out} versus V_{in} plots for extreme variation of circuit parameters.

Also shown in the figure is a unity-gain line (curve 3). This latter plot serves to determine required values of LPUL and *least negative down level* (LNDL) for base-input signals (and consequently collector-output signals). Unity circuit gain occurs for positive- and negative-input-signal levels at points A and B, respectively. Hence, the base-input signal to a stage must become at least as positive as V_A and at least as negative as V_B in order to provide an output signal having adequate positive- and negative-voltage levels for driving a succeeding stage. Careful selection of supply voltage and resistor values assures that the LPUL and LNDL input-signal voltages are obtained, without exceeding the MPUL and MNDL voltages.

Typical Circuit Values. Table 11-1 gives power-supply and resistor values for a saturated CMS implemented with the 2N3832 transistor. The circuit configuration is given in Fig. 11-6; each transistor is now considered to have a fan-out loading of 2. The 300-ohm value for R_3 gives a maximum collector current of approximately 7.5 ma in transistor Q_1. This current level permits the particular transistors to operate at their highest speeds. The 63- and 67-ohm values for R_1 and R_2, respectively, give collector voltages of approximately ± 0.22 volt at the collectors of Q_1 and Q_2. For an input-signal swing of ± 0.22 volt, the maximum negative value of collector-base voltage is approximately 0.44 volt.

Disadvantage of Circuit. Because of the small range of values for input- and output-voltage levels, component tolerances must be tightly controlled in the saturated CMS. Transistors must be carefully selected for V_{BE} and h_{FE} values. Resistors must have low tolerances to give the proper levels of output signal. Close tracking of similar components is essential over the operating-temperature range.

The above circuit restrictions can be eased considerably by the addition of emitter-follower stages at the output terminals of a saturated CMS. A new CMS configuration, referred to as "emitter-coupled logic" (ECL), is obtained in this manner. The ECL stage has largely superseded the saturated CMS in high-speed logic applications. A description of ECL is given in the following section.

Table 11-1. Circuit Values for Saturated CMS

Q_1, Q_2	2N3832
R_1	63 ohms
R_2	67 ohms
R_3	300 ohms
V_{CC}	0.25 volt
$-V_{EE}$	−3.0 volts

11-6. EMITTER-COUPLED LOGIC (ECL)

Figure 11-13 shows a circuit configuration of the ECL stage. The circuit consists of a saturated CMS having emitter-follower output stages. These emitter-follower stages provide current gain to permit greater fan-out loading; also, the emitter-follower transistors give a downward shift in output voltage from that of the saturated CMS alone. One addi-

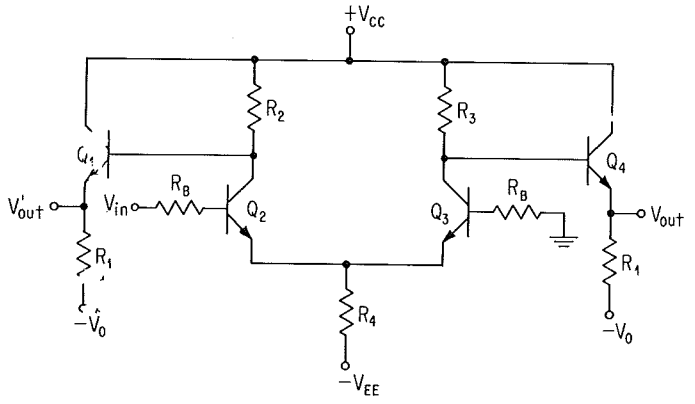

Fig. 11-13. ECL circuit configuration.

tional feature of the emitter-follower output stages is that wired-OR logic can be obtained without additional circuitry. This logic connection, described in Sec. 10-10, is achieved by wiring together two or more emitter-follower output transistors at their emitter terminals.

Base-input resistors to Q_2 and Q_3 are often required to prevent high-frequency oscillations of the above ECL stage. Insofar as the base terminals of Q_2 and Q_3 are concerned, these devices are connected in the emitter-follower configuration. The discussion in Sec. 8-2 pointed out that the emitter-follower transistor has a tendency to oscillate when driven from a low output-impedance stage. The ECL input transistors are driven from low output-impedance emitter-follower stages of a preceding ECL circuit; hence, oscillations may occur when input lines are slightly inductive or when the ground plane contains some inductance. The base-input resistors R_B in Fig. 11-13 generally have nominal values of 50 to 100 ohms. These input resistors have a negligible effect upon dc operation of the ECL stage and are neglected in any dc analysis of the circuit.

At an ambient temperature of $+25°C$, the ECL stage is able to sustain input- and output-voltage swings of approximately ± 0.4 volt. Because output voltages are taken from the emitter-follower transistors, collector voltages of Q_2 and Q_3 in Fig. 11-13 are approximately 0.75 volt more positive than the corresponding output-voltage levels. Hence, when the input signal to Q_2 is at a level of $+0.4$ volt, collector voltage of this device is at an approximate level of $+0.35$ volt, to give an output voltage of -0.4 volt at the emitter of Q_1. The V_{CB} level for Q_2 is now -0.05 volt; there is no forward current flow across the collector-base diode, and the transistor does not exhibit storage effects.

Collector supply voltage of the present circuit must be at a minimum level of approximately 1.2 volts, as contrasted to a minimum level of approximately 0.22 volt for the saturated CMS. Because of the higher V_{CC} voltage for the ECL stage, and also because of the larger output-voltage swing, tolerances upon variations of supply voltages and component values are now less stringent than they were for the saturated CMS circuit.

Graphical Analysis. Steady-state circuit analysis is similar to that described

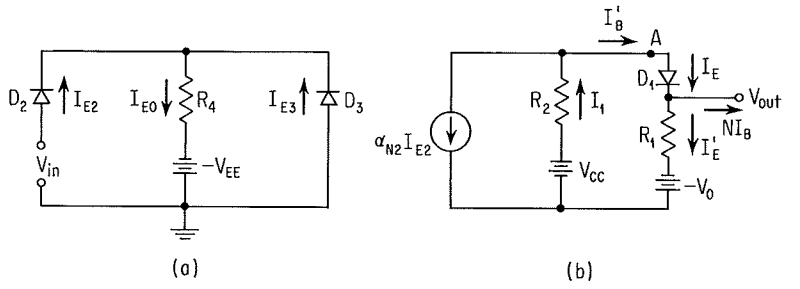

Fig. 11-14. Equivalent circuits for analyzing ECL stage of Fig. 11-13. *(a)* **Input circuit;** D_2, D_3 **are base-emitter diodes of** Q_2 **and** Q_3, **respectively, in Fig. 11-13;** *(b)* **output circuit;** D_1 **is base-emitter diode of** Q_1 **in Fig. 11-13;** $\alpha_{N2}I_{E2}$ **is collector-current generator of** Q_2.

previously for the saturated CMS. The analysis must now be extended, however, to include the emitter-follower stages. Figure 11-14 shows the two dc equivalent circuits to be used in the present analysis. Figure 11-14*a* is identical to Fig. 11-7, as input portions of the modified CMS and ECL circuits are identical. The procedure for determining diode currents in Fig. 11-14*a* is the same as that described in conjunction with Fig. 11-7. Values of I_{E2} and I_{E3} are obtained for various levels of V_{in} and retained for later use.

Figure 11-14*b* shows a dc equivalent circuit for one output side of the ECL stage.* The collector-current generator is shown as $\alpha_{N2}I_{E2}$, and base current to N fan-out loads is represented by NI_B. Analysis of the present circuit is similar to that described in Sec. 8-4 for the circuit of Fig. 8-16. In Fig. 11-14*b*, an output-voltage level is assumed, and current through R_1 is calculated. This current is added to NI_B to obtain total emitter current I_E. From a knowledge of the I_E versus V_{BE} characteristic of the device, voltage at point A can be determined. Current I'_B is obtained by dividing the I_E value by h_{FE} of the emitter-follower transistor. Current I_1 is determined from the voltage drop across R_2. The required level of $\alpha_{N2}I_{E2}$ is obtained by subtracting I'_B from I_1.

At this point, it is necessary to correlate $\alpha_{N2}I_{E2}$ with a V_{in} level of the ECL stage. The $\alpha_{N2}I_{E2}$ value determined above is divided by α_N of Q_2 to yield I_{E2}. From the previous analysis of the circuit in Fig. 11-14*a*, values of I_{E2} were obtained for various assumed levels of V_{in}. By interpolating between points in the above listing of I_{E2} versus V_{in}, the required value of V_{in} to give the calculated level of I_{E2} is obtained. As I_{E2} was determined for an assumed level of V_{out}, corresponding values of V_{in} and V_{out} are now known. Repetition of the above procedure for various assumed values of V_{out} will yield a list of V_{in} versus V_{out} for the ECL stage. Plots of V_{in} versus V_{out} are similar to those shown in Fig. 11-11 for the saturated CMS. However, output-voltage swings are larger for the ECL circuit.

Design Analysis. The ECL stage is designed from a consideration of transient response as well as dc characteristics. Two types of switching-speed measurements are made before any dc design is begun. These tests measure propagation

* The left side of the ECL circuit of Fig, 11-13 is shown. The current generator corresponds to transistor Q_2, and the diode corresponds to the base-emitter diode of transistor Q_1. An identical circuit is used for the right side of the ECL stage.

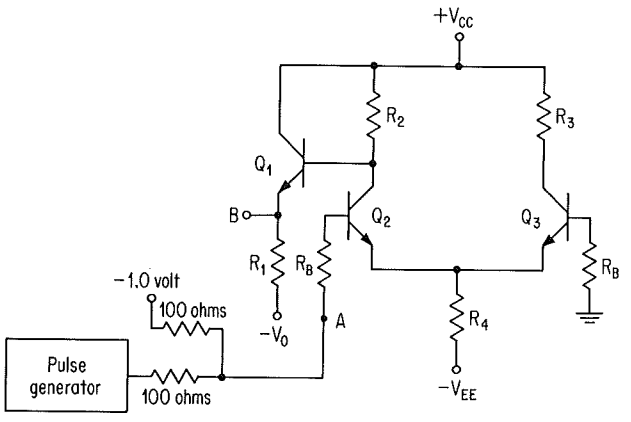

Fig. 11-15. Test circuit for measuring turnoff propagation delay t_{p2}.

delay, i.e., the time interval between a given point on the input-voltage waveform and the corresponding point on the output-voltage waveform. For convenience, the measurement can be made at the points where input and output waveforms cross the zero-voltage line. Turn-on and turnoff propagation delays are referred to as t_{p1} and t_{p2}, respectively.

The first of the ac tests is a measure of t_{p2} versus V_{CB} of the input transistor. Figure 11-15 shows a circuit configuration for this test. The pulse generator and input resistor network provide an input signal which can be varied in a positive direction to any convenient level. The negative-input signal remains at a level of -0.5 volt. The pulse generator is adjusted to give a positive level of input signal, and the turnoff propagation delay is measured between terminals A and B. A dc voltage equal to the positive-input signal is then applied to terminal A, and V_{CB} of Q_2 is measured. The above procedure is repeated for various values of positive-input signal. This yields a plot of t_{p2} versus V_{CB}; a plot of this type is shown in Fig. 11-16 for the 2N3832 transistor. As V_{CB} becomes more negative than approximately 0.5 volt (in Fig. 11-16), the transistor begins to saturate

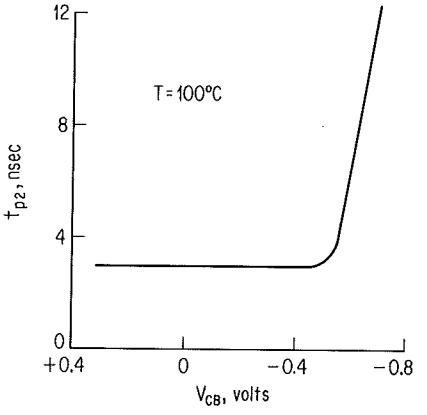

Fig. 11-16. t_{p2} versus V_{CB} for 2N3832 transistor.

heavily, and storage time becomes excessive. This test should be performed at the highest anticipated operating temperature.

A second ac test involves a measure of average propagation delay versus emitter current of the CMS proper (neglecting emitter currents of the emitter-follower stages). This is accomplished with the test circuit shown in Fig. 11-17. A load of one ECL stage is connected to the circuit under test. Emitter-current levels of Q_2 and Q_3 in the circuit under test are varied, while maintaining constant input- and output-voltage swings for this circuit. The voltage swings are kept constant so that any variation in propagation delay will be caused solely by varying the current levels in Q_2 and Q_3 and not by any changes in drive signal to either the circuit under test or the load stage.

Emitter current, and consequently collector current, of the circuit under test is varied by changing the value of R_E. Maximum emitter current of either Q_2 or Q_3 is given approximately by

$$I_{E(\max)} = \frac{V_{EE}}{R_E} \tag{11-11}$$

Collector current in each of the above devices is given by the product $\alpha_N I_E$. Thus, from Eq. (11-11), maximum collector current can be expressed

$$I_{C(\max)} = \frac{\alpha_N V_{EE}}{R_E} \tag{11-12}$$

The change in collector voltage of a transistor can be written

$$\Delta V_C = (I_{C(\max)} - I_{C(\min)})R_L \tag{11-13}$$

where $I_{C(\min)}$ is the minimum value of collector current. Substitute the right side of Eq. (11-12) for the $I_{C(\max)}$ term in Eq. (11-13). In addition, neglect the $I_{C(\min)}$ term (which is close to zero) in the latter expression. This yields

$$\Delta V_C = \frac{\alpha_N V_{EE} R_L}{R_E} \tag{11-14}$$

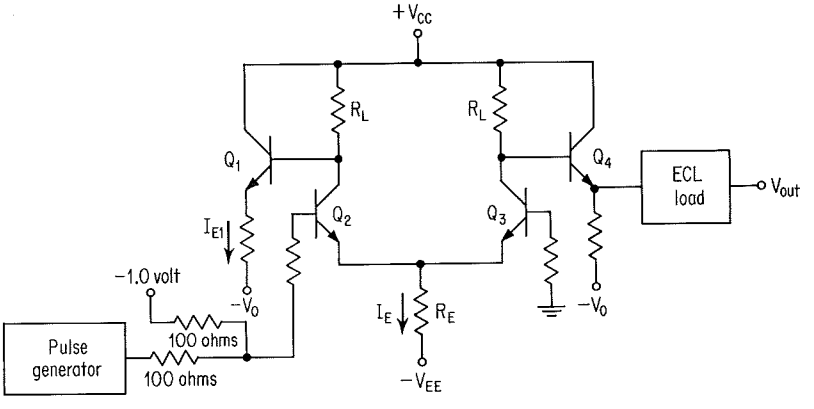

Fig. 11-17. Test circuit for measuring average propagation delay t_p.

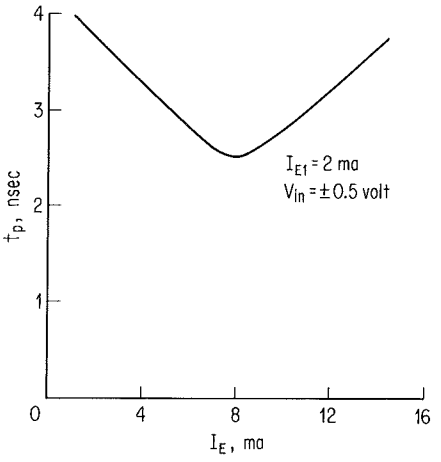

Fig. 11-18. t_p **versus** I_E **for 2N3832 transistor in ECL stage.**

Equation (11-14) shows that output-voltage swing of the circuit under test is kept constant by maintaining a constant ratio for R_L/R_E.

Propagation delays for the entire circuit of Fig. 11-17 are measured for various values of R_E. The constant turn-on and turnoff propagation delays of the load circuit are subtracted from the above measured values to yield t_{p1} and t_{p2} for the circuit under test. These two delay times are then averaged, and the resulting delay time t_p is plotted versus I_E. Current I_E is measured for a positive input signal of 0.5 volt to the base of Q_2. A typical plot of this type is given in Fig. 11-18 for the 2N3832 transistor. This latter figure shows that t_p at first decreases and then increases as I_E is increased from a low value.

At low levels of I_E in the circuit under test, t_p is circuit-limited. Transistor internal capacitances and load capacitance are initially charged by relatively small emitter and collector currents. As I_E increases, circuit capacitances are charged more quickly. In addition, as pointed out in the discussion of Sec. 2-3, emitter transition capacitance C_{te} decreases and internal cutoff frequency ω_a increases as I_E is made larger. The increase in I_E and improvement in transistor ac parameters cause the initial decrease in t_p. As I_E becomes relatively large, however, transient response of the circuit begins to degrade. This is a result of a decrease in width of the depletion layer at the collector-base junction and a consequent widening of the base region.[7] The increase in base width causes a reduction in f_T of the transistor, and transient response begins to fall off.

Plots of the type shown in Fig. 11-18 can be obtained for several values of quiescent emitter current in the emitter-follower stages. The current is measured in Q_1 of Fig. 11-17 for a positive-input signal to the base of Q_2. In general, as this current is increased, the entire plot will be found to lie closer to the horizontal axis. At large values of emitter-follower current, however, there will be no further decrease in t_p. The designer must decide how much power dissipation he is willing to trade off against a decrease in propagation delay. Regardless of current levels through the emitter-follower stages, the minimum t_p should always occur at very nearly the same level of I_E (for the CMS proper).

Results of the above ac tests are incorporated into circuit design of the ECL stage. The t_{p2} versus V_{CB} plot shows the most negative collector-base voltage at which the input transistor can be operated. This voltage should not be exceeded in the actual circuit. Plots of t_p versus I_E, for various values of emitter-follower current, show the propagation delay one can expect for given levels of I_E and emitter-follower current; conversely, if a given t_p is desired, the plots give the required values of quiescent currents.

In order to perform a graphical analysis of a proposed ECL circuit, it is necessary to have data concerning the V_{BE} versus I_E and h_{FE} versus I_E characteristics of the transistors to be used. Because of a normal variation in characteristics between individual transistors, one may be tempted to apply a worst-case design procedure to the ECL stage. A design of this type is not recommended for the present circuit, as it is likely that no circuit values exist which will permit the ECL stage to function under worst-case conditions. Rather, a statistical-design procedure, similar to the one described in Sec. 10-5, should be used for the ECL stage.

Distributions of parameters are required for a statistical design. The V_{BE} versus I_E and h_{FE} versus I_E plots may have a different distribution for each level of I_E. As it is not practical to utilize many different distributions, only the distribution of values at one level of I_E is to be used; a reasonable choice for this I_E level is one-half the maximum quiescent value of I_E.

A statistical-design procedure requires that thousands of circuits be simulated and the operating characteristics determined for each circuit. As a graphical analysis of the ECL circuit is a time-consuming task, the use of a digital computer is suggested. The graphical method of analysis described earlier involves the following three operations:

1. Algebraic addition of current levels.
2. Algebraic addition of voltage levels.
3. Determination of the point of intersection for two *VI* plots.

A digital computer can be programmed to obtain graphical solutions for current and voltage levels in a given ECL circuit. The computer program can also permute all parameters and give a weighting factor to each value of a parameter. In this manner, the computer can provide distributions of output voltage versus input voltage for the various simulated circuits. The following discussion describes one method of designing the ECL stage. It is tacitly assumed that a digital computer is available to determine operating conditions of the various circuits.

As in any circuit design, a starting point is required. The procedure is to determine nominal values of components which are likely to provide a suitable circuit yield. These component values are then fed into the computer and certain of the variables are permuted. From the results of a computer run, one or more of the components is given a slightly different nominal value, and another set of calculations is obtained. In this manner, component values can be determined for optimum circuit yield. The step-by-step procedure described below illustrates a method by which an ECL stage can be designed. Characteristics of the 2N3832 transistor are used in the design analysis. The circuit configuration is given in Fig. 11-13.

Step 1. Select V_{CC} and $-V_{EE}$. A survey of existing ECL circuits shows that V_{CC} and $-V_{EE}$ are typically 1.25 and -3.0 volts, respectively. The 1.25-volt level for V_{CC} is reasonable, as shown by the following discussion of the circuit of Fig. 11-13. The emitter of Q_1 is approximately 0.7 volt less positive than the collector of Q_2. For Q_2 at cutoff, and negligible current flow through R_2, the collector of Q_2 is at a level of 1.25 volts; consequently, the emitter of Q_1 is at a potential of 0.55 volt. Actually, as a result of a finite base current to Q_1, emitter voltage of Q_1 is typically at a level of 0.5 volt. This magnitude of positive output signal is considerably larger than the 0.2 volt or so required to turn on a succeeding stage. A suitable noise immunity is thus provided by the 1.25 volt V_{CC} supply. In addition, as will be shown later, the most negative level of output signal is approximately -0.5 volt. Hence, the output-signal swing is approximately symmetrical about ground potential.

Experience with the ECL circuit has shown that a $-V_{EE}$ level of -3 volts is suitable for maintaining an approximately constant current at the common-emitter junction of Q_2 and Q_3. A more negative voltage than -3 volts can be used for $-V_{EE}$, of course, but this increases power dissipation of the circuit.

The suitability of 1.25 volts for V_{CC} and -3 volts for $-V_{EE}$ has been described above. Hence, these voltage levels are used in the present design analysis.

Step 2. Select R_1 and V_0. From the plots of t_p versus I_E for various values of emitter-follower current, a dc level of emitter current for the emitter-follower transistor is selected to provide the desired circuit speed. This emitter current was determined for Q_1 of Fig. 11-17 with Q_2 fully on. Hence, emitter voltage of Q_1 is at approximately -0.5 volt, and emitter current of this device is given by

$$I_{E1} = \frac{V_0 - 0.5}{R_1} \tag{11-15}$$

where I_{E1} is the emitter current of Q_1. In order to minimize the number of power supplies, the $-V_0$ level in Fig. 11-13 is made equal to $-V_{EE}$. Hence, a single -3-volt supply is used for $-V_0$ and $-V_{EE}$. Substitute 3 for V_0 in Eq. (11-15), and solve the resulting expression for R_1; this yields

$$R_1 = \frac{2.5}{I_{E1}} \tag{11-16}$$

The desired level of I_{E1} is substituted into Eq. (11-16), and R_1 is determined. Let us assume that I_{E1} is equal to 2 ma; this gives a level of 1.25 kilohms for R_1.

Step 3. Select R_4. The value of R_4 determines quiescent emitter current of the ECL stage. Emitter current of Q_2 can be described by

$$I_{E2} = \frac{V_{\text{in}} - V_{BE2} + V_{EE}}{R_4} \tag{11-17}$$

where I_{E2} = emitter current of Q_2

V_{BE2} = base-emitter forward-voltage drop of Q_2

This expression can be solved for R_4, to yield

$$R_4 = \frac{V_{\text{in}} - V_{BE2} + V_{EE}}{I_{E2}} \tag{11-18}$$

From the plot of t_p versus I_E in Fig. 11-18, the optimum value of I_{E2} is seen to be approximately 7.8 ma for a 2N3832 transistor. The V_{in} level to substitute into Eq. (11-18) corresponds to the maximum positive level of V_{in} used to obtain the t_p versus I_E plot. The value of V_{BE2} is determined from a plot of I_E versus V_{BE} for the particular transistor used in the circuit. For the present analysis, a level of +0.5 volt is used for V_{in}, and I_{E2} is selected to be 7.8 ma. In addition, $-V_{EE}$ is considered to have a value of −3 volts, and V_{BE2} has a typical value of 0.82 volt. Substitution of the above values into Eq. (11-18) gives a value of 344 ohms for R_4.

Step 4. Select R_2 and R_3. The out-of-phase output-voltage level of the ECL stage is described by

$$V'_{\text{out}} = V_{C2} - V_{BE1} \tag{11-19}$$

where V'_{out} = emitter voltage of Q_1
V_{C2} = collector voltage of Q_2
V_{BE1} = base-emitter voltage of Q_1

An expression for V_{C2} can be written

$$V_{C2} = V_{CC} - (\alpha_{N2} I_{E2} + I_{B1}) R_2 \tag{11-20}$$

where α_{N2} = common-emitter forward collector-current gain of Q_2
I_{E2} = emitter current of Q_2
I_{B1} = base current of Q_1

Substitute the right side of Eq. (11-20) for V_{C2} in Eq. (11-19), and solve the resulting expression for R_2; this yields*

$$R_2 = \frac{V_{CC} - V'_{\text{out}} - V_{BE1}}{\alpha_{N2} I_{E2} + I_{B1}} \tag{11-21}$$

The most negative level of V'_{out} is nominally −0.5 volt at +25°C and occurs when I_{E2} is at the 7.8-ma level used to solve Eq. (11-18). At the +25°C operating temperature, V_{BE1} has a nominal value of 0.75 volt. The 2N3832 transistor has a typical h_{FE} of 30 at 7.8 ma of collector current; hence, a value of $^{30}/_{31}$ is used for α_{N2} in the above expression. Emitter current of Q_1 is given by

$$I_{E1} = \frac{3 - V'_{\text{out}}}{R_1} \tag{11-22}$$

Substitution of values into Eq. (11-22) gives a level of 2.0 ma for I_{E1}. This 2.0-ma level is divided by h_{FE} of Q_1 to obtain I_{B1}. For the present analysis, h_{FE} is considered to have a value of 30 at the 2.0-ma level of emitter current. This gives a value of 0.07 ma for I_{B1}. All values on the right side of Eq. (11-21) are now known; R_2 is calculated to be 131 ohms.

When transistor Q_3 is fully on, emitter current of this device is slightly smaller than I_{E2}. Consequently, let R_3 be 5 per cent larger than R_2; this gives a value of 138 ohms for R_3.

Step 5. Permute Circuit Values; Determine Circuit Yield. Using the above circuit values, together with distributions of transistor and resistor characteristics, the computer simulates several hundred circuits. Distributions of V_{BE} versus I_E,

* The positive or negative sign associated with V_{out} must be used in Eq. (11-21).

h_{FE} versus I_E, and of resistor values are used in the above simulation. Power-supply voltages are taken at their *worst-case* levels, as there is no actual distribution associated with these voltages. For each simulated circuit, V_{in} is assigned several values of negative and positive voltage levels. The computer determines both the true and complementary output-voltage levels for each value of V_{in}. In order for a circuit to be considered useful, the following inequalities must be satisfied

$$\left|\frac{V'_{\text{out}}}{V_{\text{in}}}\right| \geqslant 1 \tag{11-23}$$

$$\left|\frac{V_{\text{out}}}{V_{\text{in}}}\right| \geqslant 1 \tag{11-24}$$

where V_{out} is the emitter voltage of Q_4. In addition, saturation of the circuit must be avoided; this is accomplished if *

$$V_{C2} - V_{\text{in}} > V_{CB(\text{sat})} \tag{11-25}$$

where $V_{CB(\text{sat})}$ is the most negative allowable value for V_{CB} as determined from a plot of the type shown in Fig. 11-16. If the above three inequalities do exist, the circuit is considered valid.

By compiling the number of valid circuits for each value of V_{in}, the computer can provide a listing of probability of valid circuits for various values of V_{in}. These results can be plotted to obtain LPUL, MPUL, LNDL, and MNDL for the proposed circuit design. Consider that the plots in Fig. 11-19 represent data generated by the computer. Figure 11-19*a* shows positive-input voltages versus circuit yield, and Fig. 11-19*b* shows negative-input voltage versus circuit yield; plots are given for the two extremes of temperature operation, -40 and $+100°C$ for the present example. Suitable choices for LPUL and MPUL are shown in Fig. 11-19*a*. The LPUL is determined from the $-40°C$ plot at a point where circuit yield reaches a nearly constant maximum value. The MPUL is selected as the V_{in} level beyond which the $+100°C$ plot begins to show a significant decrease in circuit yield. Choices for LNDL and MNDL are shown in Fig. 11-19*b*. The

* The positive- or negative-voltage levels associated with V_{C2} and V_{in} must be used in Eq. (11-25).

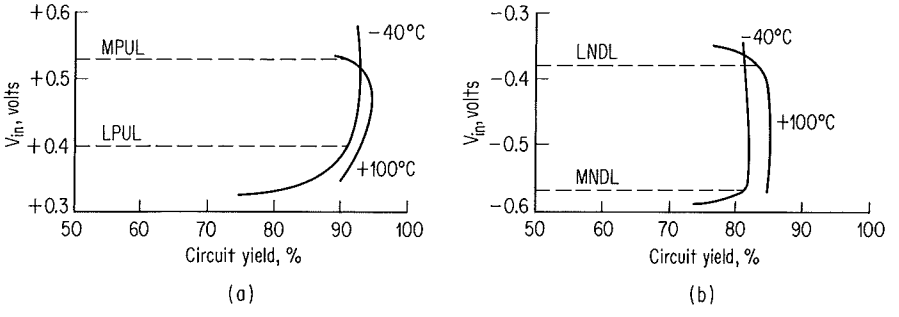

Fig. 11-19. Plots of V_{in} versus circuit yield for *(a)* positive-input voltage and *(b)* negative-input voltage.

LNDL is determined from the $+100°C$ plot, and the MNDL is determined from the $-40°C$ plot.

If it is determined that circuit yield is too low for the above nominal values of resistances, the designer can permute R_2, R_3, R_4, or V_{CC} and again determine circuit yield. In addition, he can permute various combinations of the above four parameters and obtain circuit yield for each combination of parameters.

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12

Flip-flop Circuits

12-1. FLIP-FLOP OPERATION

Two inverter stages, cross-coupled as shown in Fig. 12-1, provide a basic form of bistable multivibrator, or "flip-flop," circuit. The above circuit may be analyzed by redrawing it as in Fig. 12-2, which shows that the flip-flop is simply a connection of two TRL NOR stages, with the output of each stage serving as the input to the other stage. When transistor Q_1 is at cutoff, voltage at point A is sufficiently positive to saturate transistor Q_2. Voltage at point B is now slightly negative, and Q_1 is reverse-biased to cutoff. The above operating conditions for Q_1 and Q_2 represent one stable state of the flip-flop. A second stable state exists when Q_1 is in saturation and Q_2 is at cutoff.

A transition of the flip-flop from one stable state to the other can be induced by any one of several different techniques. Consider, for instance, that the flip-flop circuit of Fig. 12-1 is at the stable state where Q_1 is on and Q_2 is off. The circuit will change to the other stable state (Q_1 off and Q_2 on) for any one of the following:

1. Disconnect Q_1 from the circuit and then reconnect it. (This causes Q_2

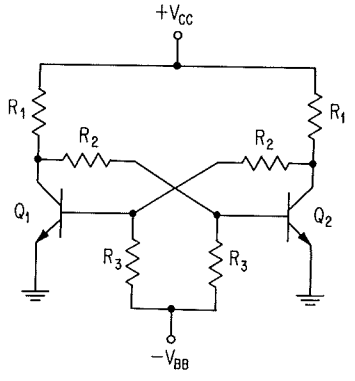

Fig. 12-1. Basic flip-flop circuit.

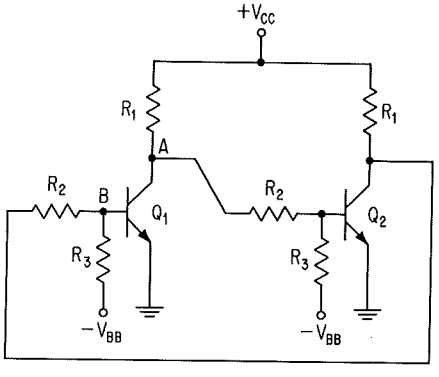

Fig. 12-2. Basic flip-flop redrawn as two TRL stages.

to turn on. When Q_1 is again connected, the $V_{CE(sat)}$ collector voltage of Q_2 prevents Q_1 from turning on.)

2. Apply a positive-voltage level to the base of Q_2. (Q_2 turns on, and Q_1 turns off.)
3. Apply a negative-voltage level to the base of Q_1. (Q_1 turns off, and Q_2 turns on.)
4. Temporarily ground the collector of Q_2. (This removes the base drive to Q_1, and the base of Q_2 becomes forward-biased.)
5. Connect a low resistance from the collector of Q_1 to the $+V_{CC}$ supply. (The increase in collector current forces Q_1 out of saturation.)

Methods 1 and 5 are not practical for most circuit applications of the flip-flop. The techniques described in 2 to 4 are widely used to change the operating state of a flip-flop, and they will be covered in greater detail throughout this chapter.

Small capacitors are often connected across the R_2 resistors in Figs. 12-1 and 12-2. These capacitors serve to couple a positive- or negative-going signal from the collector of one transistor to the base of the other transistor. Transient response of the circuit is improved considerably by use of the above speedup capacitors.*

Cross-coupled single-input NOR stages are used in the above flip-flop circuit. A logic-circuit representation of this flip-flop connection is shown in Fig. 12-3; symbols for the OR and NOT (invert) operations are indicated in the figure. The present flip-flop is shown to consist of single-input OR gates, followed by inverter stages, with the output of each inverter cross-coupled to an OR-gate input. This form of basic flip-flop is referred to here as a NOR-type flip-flop.

Flip-flop stages can also be constructed with AND-NOT logic as shown in the diagram of Fig. 12-4; the stage is considered to be a NAND-type flip-flop. This circuit configuration can be implemented by cross-coupling single-input DTL NAND gates of the type described in Sec. 10-6.

Any of the inverter circuits described in Chap. 10 can be used to form a flip-flop stage. The current-mode switching circuits described in Chap. 11 can also be connected as flip-flop elements. The most popular forms of flip-flop circuits are modifications to the circuit shown in Fig. 12-1. Hence, the following discus-

*The discussion in Sec. 6-7 describes the effect of these speedup capacitors.

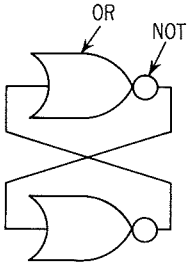

Fig. 12-3. Logic-circuit diagram for NOR-type flip-flop.

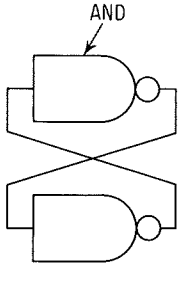

Fig. 12-4. Logic-circuit diagram for NAND-type flip-flop.

sions of flip-flop operation and design are concerned principally with cross-coupled TRL NOR stages. Many of the principles described are directly applicable to other forms of flip-flop circuit.

12-2. BINARY STORAGE

Because of its ability to remain indefinitely in either one of two stable states, the flip-flop is able to store information. The two output levels of a flip-flop are complements of each other and can be used to represent the binary numbers 1 and 0. Positive logic will be used throughout this chapter; a relatively positive output signal and a relatively negative output signal are regarded as binary 1 and binary 0, respectively. One output terminal of the flip-flop is considered to provide the true output signal, whereas the other output terminal provides the complementary, or false, output signal. Input signals from control circuitry are used to change the state of a flip-flop. In this manner, the information content of a flip-flop can be changed from 1 to 0, or vice versa.

Various input-circuit logic schemes can be employed to control the state of a flip-flop; this allows several different logical relationships to exist between input and output signals of a stage. The flip-flop circuits described below provide various logic functions. These functions are determined by the choice of input circuitry to the basic flip-flop configuration of Fig. 12-1.

12-3. SET-RESET FLIP-FLOP

Figure 12-5 shows a flip-flop having two input-signal lines. The output terminals of this circuit are shown as P (true) and $\bar{P}$ (complement). When Q_1 is on, voltage at P is positive and represents a binary 1; the circuit is now considered to be storing a 1. For Q_2 turned on, voltage at P is close to ground potential, and the circuit stores a 0.

The two input-signal lines to the above flip-flop are designated *set* and *reset.*[1] Consider that the set line is at the $+V$ level and that the reset line is held at

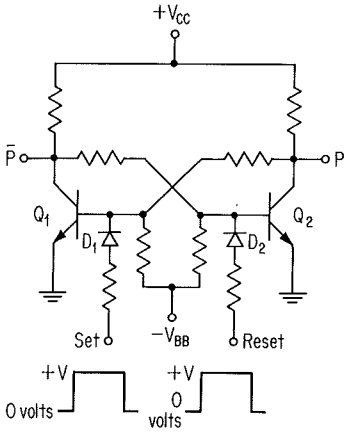

Fig. 12-5. Diode-coupled *SR* flip-flop for positive-input signals.

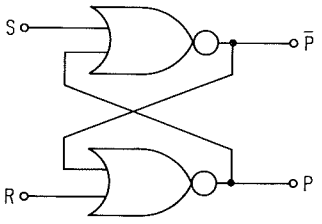

Fig. 12-6. Logic-circuit diagram for *SR* flip-flop of Fig. 12-5.

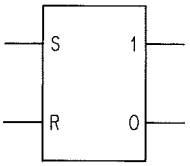

Fig. 12-7. Symbol for *SR* flip-flop of Fig. 12-5.

ground potential. Diode D_1 is forward-biased and provides base current to Q_1; this transistor is in saturation, and P is at a positive voltage level. The circuit is presently *set* to the 1 state. If the input signal is reduced to ground potential, the flip-flop continues to store a 1. If the reset line is then energized with the $+V$ level and the set line remains at ground potential, diode D_2 provides forward base current to Q_2; this transistor turns on, and the flip-flop changes state. The flip-flop is now *reset,* or cleared, to the 0 state. This last stable state is maintained when the reset line is grounded. If both the set and reset lines are simultaneously at the $+V$ level, the final state of the flip-flop is indeterminate. Hence, only one input signal at a time can be positive. Because the present flip-flop configuration can be set to 1 and reset to 0, the circuit is generally referred to as a "set-reset" (*SR*) flip-flop. The *SR* stage is sometimes referred to as a "latch" circuit. This name results from the circuit's ability to latch in one state or the other, depending upon which of two input lines is energized.

A logic-circuit diagram of the above *SR* flip-flop is shown in Fig. 12-6. The logic configuration is identical to that of Fig. 12-3, except that each OR gate now has *two* input terminals. The added input terminal at each gate allows external signals to change the state of the circuit.

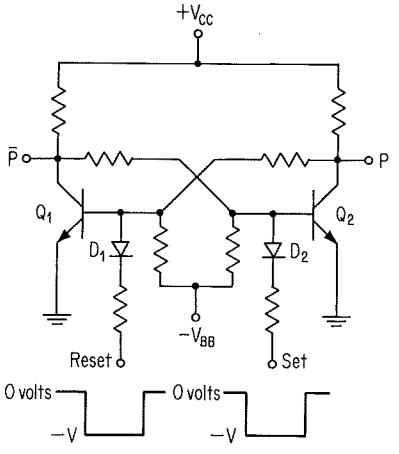

Fig. 12-8. Diode-coupled *SR* flip-flop for negative-input signals.

Figure 12-7 shows a symbol for the NOR-type *SR* flip-flop described above. The output lines are shown to have the binary values associated with the storage of a 1.* These output binary levels are reversed when a 0 is stored in the flip-flop.

Negative-input signals may also be used to set and reset the basic flip-flop of Fig. 12-1; this is shown in the circuit diagram of Fig. 12-8. A negative-input voltage to either diode is coupled to the base of the associated transistor. As an N-P-N transistor cannot be on when its base-emitter voltage is negative, the ON transistor is turned off by a negative-input signal to the proper diode. In the present circuit,

*This assignment of output values will be used whenever a flip-flop symbol is shown.

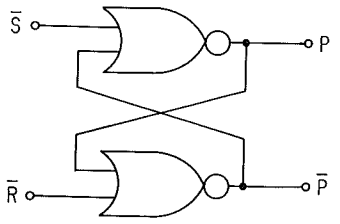

Fig. 12-9. Logic-circuit diagram for *SR* flip-flop of Fig. 12-8.

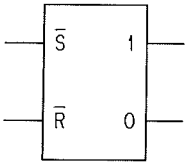

Fig. 12-10. Symbol for *SR* flip-flop of Fig. 12-8.

the flip-flop is set when a negative signal is applied to D_2 and is reset when the input signal to D_1 is negative. Circuit operation is indeterminate if both set and reset input lines are simultaneously negative.

Figures 12-9 and 12-10 respectively show the logic-circuit diagram and the symbol for the *SR* flip-flop of Fig. 12-8. The set and reset input signals are shown inverted, as the *complements* of these signals actually set or reset the circuit.

One popular form of *SR* stage is shown in Fig. 12-11. The collectors of transistors Q_3 and Q_4 are wired to the collectors of transistors Q_1 and Q_2, respectively. When a positive-input signal is applied to the base resistor of Q_3, the $\bar{P}$ output is at a $V_{CE(\text{sat})}$ level; this prevents the base of Q_2 from being forward-biased, and the flip-flop stores a 1. Conversely, Q_1 cannot be forward-biased when the base-input signal to Q_4 is positive; the flip-flop now stores a 0. Transistors Q_3 and Q_4 are often referred to as "pullover transistors," as they are able to pull down the output voltage and thus control the state of the flip-flop. The present circuit is set by application of a $+V$ level to the base-input resistor of Q_3 and is reset when the $+V$ level is applied to the base-input resistor of Q_4. The circuit does not operate properly if set and reset inputs are simultaneously at the $+V$ level.

The logic-circuit diagram and the symbol for the latter flip-flop stage are identical to that associated with the diode-coupled *SR* flip-flop of Fig. 12-5.

DC input-voltage levels are used for the above *SR* flip-flops. Other flip-flop circuits, described later, are able to change state only when a pulse-type input

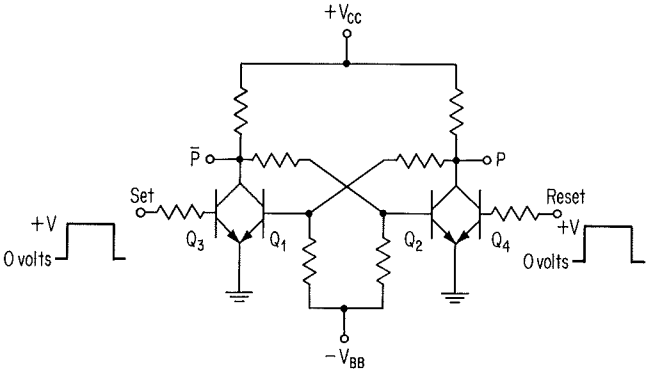

Fig. 12-11. *SR* flip-flop with pullover transistors.

signal is used. It will then be convenient to incorporate the physical quantity *time* in a discussion of circuit operation. In order to provide a common basis for comparison of various types of flip-flop circuits, the following discussion introduces the time element into an analysis of *SR* flip-flop operation.

Logically speaking, there is no difference between the *SR* flip-flops of Figs. 12-5 and 12-11. The circuit of Fig. 12-8 is logically identical to the above stages provided that *negative* logic is used and the set and reset terminals are interchanged. For purposes of analysis, only the *SR* flip-flop of Fig. 12-5 is considered. It is to be understood, however, that the final logical results apply equally well to the *SR* flip-flops of Figs. 12-8 and 12-11 (with the above logic modifications made to the circuit of Fig. 12-8).

Figure 12-12 shows two diode AND gates, together with input-and output-voltage waveforms. Input signals S' and R' are ANDed with clock-pulse W; the resulting output waveforms take on positive voltage levels only when both input signals to the corresponding AND gate are at a positive voltage level. Thus, input-signal levels S' and R' are gated to appear as output signals S and R, respectively. These output signals are used as set and reset inputs to the *SR* flip-flop. The entire flip-flop stage is now referred to as a "clocked *SR* flip-flop."

For any flip-flop, there is a certain time delay between application of an input signal and its effect upon the state of the flip-flop. This delay is referred to as the "transition time" of the circuit, i.e., the time required to change the state of the flip-flop. The clock-pulse signal described above has a period which is greater than the transition time of the stage. Hence, sufficient time is allowed for the flip-flop to change state between successive S and R signals. The S and R signals do not vary during the 1 state of the clock pulse.

Because the S and R signals can now appear only at given times, it is possible to write a truth table relating the input-signal levels at time t_n to the output-signal levels at time t_{n+1} (one time interval later than t_n). Time is referenced to the *leading* edge of the clock-pulse signal. For instance, at time t_2 in Fig. 12-12, S' is positive and R' is at ground potential; this causes S to be positive and R to be rela-

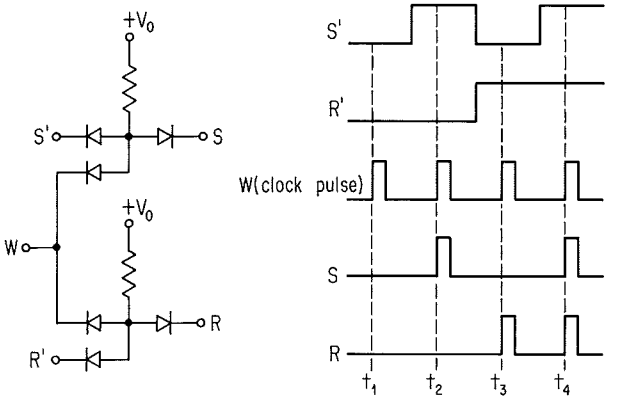

Fig. 12-12. Diode AND gates, together with waveforms showing clocked AND gating.

tively negative. Regardless of which state the flip-flop is in at t_2, the true-output line P will be positive at t_3. Table 12-1 shows a truth table for the true output of the clocked SR flip-flop.

The table indicates that for S and R equal to 0 at t_n, P has the same output at t_{n+1} as it had at t_n. This occurs because the flip-flop cannot change state when S and R are both 0. The table also shows that the output becomes indeterminate when S and R are both 1.

Table 12-1. Truth Table for True Output of Clocked SR Flip-flop

t_n		t_{n+1}
S	R	P
0	0	P at t_n
1	0	1
0	1	0
1	1	Indeterminate

Input- and output-voltage waveforms for the clocked flip-flop described above are shown in Fig. 12-13. The particular sequence of set and reset pulses is arbitrary and has no special significance. Width of the output signal is seen to be determined by the time interval between adjacent set and reset pulses.

Set and reset input signals may be capacitively coupled to either of the above SR flip-flops, as shown in Fig. 12-14. The RC circuits differentiate the square-wave input signals and provide positive- and negative-voltage spikes to the set and reset input circuits; the positive-voltage spikes are useful for setting or re-setting the flip-flops of Fig. 12-5 or 12-11, whereas the negative-voltage spikes control the state of the flip-flop of Fig. 12-8.

12-4. TRIGGER (DELAY) FLIP-FLOP

Another type of flip-flop circuit is similar to the clocked SR stage described above, except that delay elements are included between the S and R input terminals and the flip-flop itself. A logic-circuit diagram of this latter flip-flop is shown in Fig. 12-15; the circuit is sometimes referred to as a "delay," or D, flip-flop, although it is more commonly known as a "trigger," or T, flip-flop. The nature of the S and R inputs at time t_n determines whether a 1 or a 0 is to be stored at time t_{n+1}. A unique feature of the present circuit is that once the flip-flop has begun to change state, signal levels at the S and R terminals no longer have any effect upon the final state of the stage. Hence, the S and R input levels are allowed to change during the transition interval of the flip-flop. This feature, provided by the delay elements, does not exist for the clocked SR stage.

One form of trigger flip-flop is shown in Fig. 12-16.[2] Although this circuit configuration is by no means the only manner in which a trigger flip-flop can be implemented, it has been so widely used that it is a standard circuit. This circuit is seen to be derived from the basic flip-flop of Fig. 12-1.

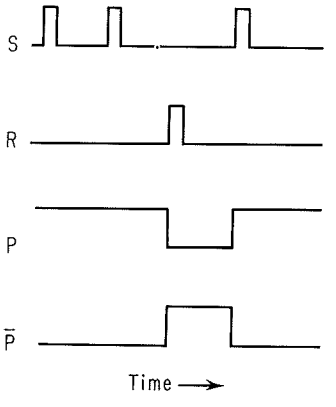

Fig. 12-13. Input- and output-voltage waveforms for clocked SR flip-flop.

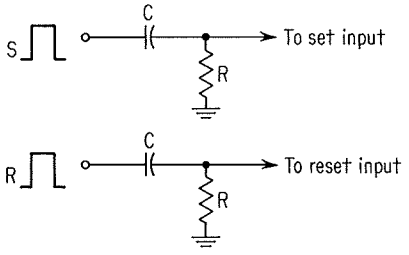

Fig. 12-14. Capacitance coupling of set and reset input pulses.

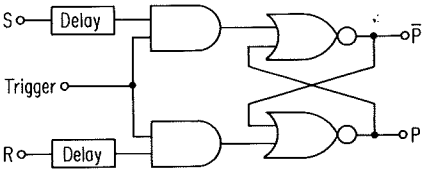

Fig. 12-15. Logic-circuit diagram for trigger flip-flop.

Consider that the circuit of Fig. 12-16 is at the stable condition where the S input is at $+V$ volts and the R input is at ground potential. The trigger-signal level is initially assumed to be at $+V$ volts. The $+V$ level at the S terminal is transmitted through resistor R_7 and appears at the cathode of diode D_3. Both sides of capacitor C_4 have equal voltages of $+V$ volts, and no charge is stored on this capacitor. On the other hand, the R terminal is at ground potential, and a voltage difference of V volts exists across capacitor C_3. This latter capacitor is charged through the conduction path consisting of diode D_1 and the grounded R terminal.

Let the trigger signal now fall instantaneously to ground potential. As the left side of C_3 was initially negative with respect to its right side (which is now at ground potential), the cathode of D_2 becomes negative with respect to ground potential. This negative-voltage level forward-biases D_2; regardless of the former

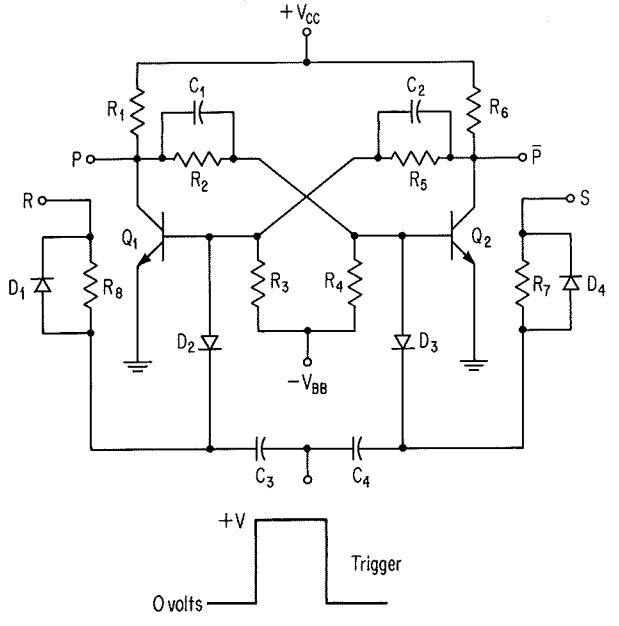

Fig. 12-16. Trigger flip-flop.

state of the flip-flop, Q_1 and Q_2 must now be at cutoff and saturation, respectively. The negative-going step of the trigger signal is also transmitted through C_4; however, the positive potential at the right side of this capacitor prevents any negative signal from appearing at the base of Q_2.

Let us consider that Q_1 had been on and is turned off by the above process. At the instant of turnoff for Q_1, the positive-going collector voltage of this transistor is coupled by capacitor C_1 into the base of Q_2; this causes Q_2 to turn on much harder than if C_1 were not present. As Q_2 turns on, its collector voltage drops toward ground potential. This negative-going voltage is transmitted by capacitor C_2 and appears at the base of Q_1 as a negative spike of voltage, thus causing Q_1 to turn off even harder. The above action is regenerative and provides a fast transition time for the stage.

A similar analysis to the above shows that if the S and R input levels are now interchanged, the circuit will trigger to its second stable state during the negative-going portion of the trigger pulse.

The foregoing analysis has considered that the S, R, and trigger signals rise to the same level of positive voltage. It is not necessary for the above voltage levels to be equal. However, if the trigger voltage is small, there may be too little negative voltage developed to turn off the conducting transistor. Also, if the trigger voltage becomes significantly more positive than the positive level of S or R, both input capacitors may simultaneously charge to voltage levels which will forward-bias both base-input diodes when the trigger signal drops to ground potential. As this would tend to turn both transistors off, the final state of the flip-flop could well be indeterminate.

Input capacitors C_3 and C_4 serve as a short-term memory during the trailing edge of the input-voltage waveform. This memory is a result of the charge stored during the positive portion of the input signal. The capacitors effectively "steer" the negative-going clock pulse to the base of the conducting transistor. It is to be noted, however, that a steering capacitor, and not the input signal, turns off the conducting transistor. In order for this turnoff to occur, the negative charge stored on the capacitor must be sufficiently large to overcome the positive base charge of a saturated transistor. Thus, a steering capacitor must have a minimum value of capacitance; the required capacitance is determined by magnitude of input voltage, by transistor type, and also by resistor values used in the collector and base circuits.

The above trigger flip-flop is able to change state only during the trailing edge of the positive-input trigger signal. If the S or R levels change during this interval, any tendency for a steering capacitor to recharge to a different voltage level is obviated by the inherent delay time required to charge a capacitor.

Figure 12-17 shows a symbol for the trigger flip-flop. The set and reset terminals are designated S_D and R_D, respectively, in order to denote that a *time delay* is associated with these terminals. The clock-pulse terminal is shown as T to indicate that the flip-flop can be *triggered* only when

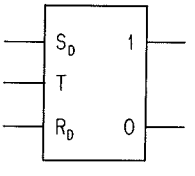

Fig. 12-17. Symbol for trigger flip-flop.

Table 12-2. Truth Table for True Output of Complementing Flip-flop

t_n	t_{n+1}
T	P
0	P at t_n
1	$\bar{P}$ at t_n

an input signal is applied to this terminal.

There is no logical difference between the trigger flip-flop and the clocked SR stage described in Sec. 12-3. Hence, the truth table of Table 12-1 is valid for the trigger flip-flop. The table shows that this latter circuit has unpredictable operation if the set and reset inputs are simultaneously at the 1 level.

12-5. COMPLEMENTING FLIP-FLOP

Let the S and R inputs of Fig. 12-16 be connected to the collectors of Q_2 and Q_1, respectively. As these two transistors have complementary outputs, one or the other of the S and R terminals is at the 1 state, with the other terminal at the 0 state. Each time the clock signal is at a positive level, the steering capacitor associated with the on transistor charges to nearly the level of clock signal. When the clock signal falls to ground potential, the flip-flop changes state. This process occurs *each* time the clock signal changes from binary 1 to binary 0.

Table 12-2 is a truth table for the above circuit configuration; the clock signal is designated T. For a 1 input on the T line at time t_n, the circuit changes, at time t_{n+1}, to the *complement* of its former state. Hence, the circuit is often referred to as a "complementing flip-flop."[3] Other names for this circuit include "binary," "toggle flip-flop," and "binary trigger circuit."

Figure 12-18 shows input- and output-voltage waveforms for the above complementing flip-flop. The output is seen to change state each time the input signal changes from 1 to 0. This results in an output signal having one-half the repetition rate of the input signal. Consequently, the complementing flip-flop is a divide-by-two stage; this is an important property of the circuit and is considered in greater detail in Chap. 13.

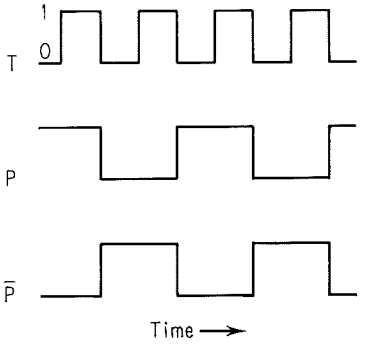

Fig. 12-18. Input- and output-voltage waveforms for circuit of Fig. 12-16 connected as a complemeniing flip-flop.

The symbol for the complementing flip-flop is identical to that given in Fig. 12-17 except that the R_D and S_D inputs are now omitted.

12-6. SET-RESET-TRIGGER FLIP-FLOP

By combining the set and reset inputs of Fig. 12-5 with the pulse-steering network of Fig. 12-16, a set-reset-trigger SRT flip-flop is obtained. The SRT stage has the truth table of either the SR flip-flop or of the T flip-flop, but *not* that of both circuits simultaneously. This is a result of the indeterminate circuit operation which may occur when a 1 is applied to either the S or R input and, at the same time, to the T input. Care must be taken to assure that only one of the S, R, or T terminals is energized at any given time.

12-7. *JK* FLIP-FLOP

The *JK* flip-flop has two inputs designated *J* and *K*. A 1 at the *J* input alone sets the flip-flop; the circuit is reset by applying a 1 to the *K* input alone. Insofar as set-reset operation is concerned, the *JK* stage is similar to the *SR* flip-flop. However, the *JK* stage has the additional feature that a 1 applied simultaneously to both the *J* and *K* inputs causes the circuit to change state. Thus, the *JK* flip-flop can be used simultaneously for both set-reset and trigger operation. Table 12-3 is a truth table for the true output of the *JK* stage.

Table 12-3. Truth Table for True Output of *JK* Flip-flop

t_n		t_{n+1}
J	*K*	*P*
0	0	P at t_n
1	0	1
0	1	0
1	1	$\overline{P}$ at t_n

The *SRT* stage can be converted to a *JK* flip-flop by use of the input logic circuitry shown in Fig. 12-19. Various combinations of the true and complemented *J* and *K* signals are gated by clock-signal *W* in AND gates A_1, A_2, and A_3. Regardless of the *J* and *K* input combinations to these gates, only one line to the flip-flop can be positive at a time. This allows the flip-flop to be set, reset, or triggered without ambiguity.

12-8. DC DESIGN OF THE FLIP-FLOP

As pointed out earlier, the basic flip-flop of Fig. 12-1 is simply a connection of two TRL stages; each stage has a fan-in and a fan-out of unity. This circuit can be designed by the worst-case method described in Sec. 10-4. However, that design technique does not readily take into account the various loads which may be placed on the flip-flop. For this reason, the following discussion presents a specific dc design method for the basic flip-flop.

Figure 12-20 shows the basic flip-flop for the condition where Q_1 is in saturation and Q_2 is at cutoff. Point *A* is at a $V_{CE(\text{sat})}$ voltage level, and external load current I_1 flows *into* this point; the circuit serves as a *sink* for the I_1 current. Voltage at point *B* is at a highly positive V_{OFF} level and external load current I_2 flows *out* of this point; the circuit is a *source* for the I_2 load current. Collector and base reverse-leakage currents are shown as I_{CEX} and I_{BX}, respectively. The remaining current designations are given merely for purposes of analysis.

A logic circuit is generally characterized electrically by its terminal current and

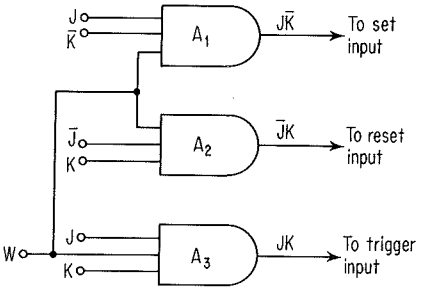

Fig. 12-19. Input circuitry for converting *SRT* flip-flop to *JK* flip-flop.

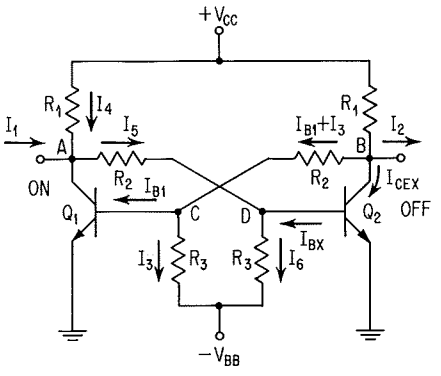

Fig. 12-20. Static circuit conditions for one stable state of basic flip-flop.

voltage ratings. Hence, for given power-supply voltages, the circuit of Fig. 12-20 is specified to have a *maximum* value of V_{ON} (corresponding to $V_{CE(sat)}$) for a given level of I_1, and a minimum value of V_{OFF} for a given level of I_2. It is assumed that V_{ON}, V_{OFF}, I_1, I_2, and supply-voltage levels are known.

For the above static conditions of the flip-flop, current through the collector resistor of Q_2 is the sum of I_2, I_{B1}, I_3, and I_{CEX}. The voltage drop caused by these currents must not reduce voltage at point B below the V_{OFF} level. Hence, R_1 is described by

$$R_1 = \frac{V_{CC} - V_{OFF}}{I_2 + I_{B1} + I_3 + I_{CEX}} \tag{12-1}$$

This last expression gives a maximum value for R_1. Collector current of Q_1 can be written

$$I_C = I_4 + I_1 - I_5 \tag{12-2}$$

or

$$I_C = \frac{V_{CC} - V_{ON}}{R_1} + I_1 - \frac{V_{BE(OFF)} + V_{ON}}{R_2} \tag{12-3}$$

Base current of the saturated transistor should be somewhat larger than I_C/h_{FE}. As pointed out in the discussion of Sec. 6-3, a useful rule of thumb is to operate the transistor at a forced gain of from 0.4 to 0.7 times the h_{FE} value listed on the data sheet; a forced gain of $0.4h_{FE}$ is used here. Base current to Q_1 is thus given by

$$I_{B1} = \frac{2.5I_C}{h_{FE}} \tag{12-4}$$

The right side of Eq. (12-1) is substituted for R_1 in Eq. (12-3) and the resulting expression substituted for I_C in Eq. (12-4); this yields

$$I_{B1} = \frac{2.5}{h_{FE}}\left[\frac{(V_{CC} - V_{ON})(I_2 + I_{B1} + I_3 + I_{CEX})}{V_{CC} - V_{OFF}} + I_1 - \frac{V_{BE(OFF)} + V_{ON}}{R_2}\right] \tag{12-5}$$

Current to the left of point B is given by

$$I_{B1} + I_3 = \frac{V_{OFF} - V_{BE(ON)}}{R_2} \tag{12-6}$$

Also, current I_3 flowing from point C can be described by

$$I_3 = \frac{V_{BB} + V_{BE(ON)}}{R_3} \tag{12-7}$$

Substitution of the right side of Eq. (12-7) for I_3 in Eq. (12-6) yields, after slight rearrangement of terms,

$$I_{B1} = \frac{V_{OFF} - V_{BE(ON)}}{R_2} - \frac{V_{BB} + V_{BE(ON)}}{R_3} \tag{12-8}$$

The right side of Eq. (12-8) is substituted for I_{B1} in Eq. (12-5). Also, the right side of Eq. (12-6) is substituted for $I_{B1} + I_{B3}$ in Eq. (12-5). Performing the above substitutions and solving for R_2 yield

$$R_2 = \frac{\int}{\varepsilon + \mu/R_3} \tag{12-9}$$

where $\int = V_{OFF} - V_{BE(ON)} - \frac{2.5}{h_{FE}}\left[\frac{(V_{CC} - V_{ON})(V_{OFF} - V_{BE(ON)})}{V_{CC} - V_{OFF}} - (V_{ON} + V_{BE(OFF)})\right]$

$$\varepsilon = \frac{2.5}{h_{FE}}\left[\frac{(V_{CC} - V_{ON})(I_2 + I_{CEX})}{V_{CC} - V_{OFF}} + I_1\right]$$

$$\mu = V_{BB} + V_{BE(ON)}$$

Current at point D is given by

$$I_6 = I_5 + I_{BX} \tag{12-10}$$

The I_6 and I_5 terms in Eq. (12-10) can be expressed in terms of voltage drops across the corresponding resistors; hence, assuming that $V_{BE(OFF)}$ is a negative quantity,

$$\frac{V_{BB} - V_{BE(OFF)}}{R_3} = \frac{V_{BE(OFF)} + V_{ON}}{R_2} + I_{BX} \tag{12-11}$$

Equations (12-9) and (12-11) can be solved simultaneously for R_3; this yields

$$R_3 = \frac{\int(V_{BB} - V_{BE(OFF)}) - \mu(V_{BE(OFF)} + V_{ON})}{\varepsilon(V_{BE(OFF)} + V_{ON}) + \int I_{BX}} \tag{12-12}$$

The above expression can be solved for R_3 and the result substituted into Eq. (12-9) to obtain R_2.

EXAMPLE 12-1

Consider that the following conditions exist for the circuit of Fig. 12-20:

$V_{CC} = +10$ volts	$I_1 = 3$ ma	$V_{BE(OFF)} = -0.2$ volt
$-V_{BB} = -10$ volts	$I_2 = 2$ ma	$I_{BX} = 2$ μa
$V_{OFF} = 3$ volts	$h_{FE} = 30$	$I_{CEX} = 1$ μa
$V_{ON} = 0.2$ volt	$V_{BE(ON)} = 0.7$ volt	

Determine resistor values for the circuit.

SOLUTION:

Step 1. Equation (12-12) is solved for R_3.

$$R_3 = 80.3 \text{ kilohms}$$

Step 2. The above value of R_3 is substituted into Eq. (12-9) and R_2 is obtained.

$$R_2 = 3.35 \text{ kilohms}$$

Step 3. From Eq. (12-6), $I_{B1} + I_3$ is determined.

$$I_{B1} + I_3 = 0.686 \text{ ma}$$

All values on the right side of Eq. (12-1) are known, and R_1 is calculated.

$$R_1 = 2.61 \text{ kilohms}$$

Many present-day transistors have extremely low leakage currents, even at elevated temperatures. Consequently, the $-V_{BB}$ supply is often omitted in the basic flip-flop stage; the base resistors are returned to ground potential instead of to $-V_{BB}$. The lack of a negative-voltage supply to provide reverse base-drive current is not important, as small capacitors can be connected across the R_2 resistors to accomplish the same purpose.

Slight modifications to the above design equations are required when $-V_{BB}$ is at ground potential. The above expressions were derived in accordance with the general practice throughout this book of substituting the absolute value of a voltage or current into an equation. The value of $V_{BE(\text{OFF})}$ was considered to be negative, and the equations involving this term were written with this in mind. However, as $V_{BE(\text{OFF})}$ must now be positive when $-V_{BB} = 0$, certain of the above expressions are no longer valid.

By performing an analysis similar to that used to obtain Eqs. (12-1) to (12-9), an expression can be written for R_2. The analysis is simplified considerably and gives a slightly more conservative design if ON-state collector current of Q_1 (refer to Fig. 12-20) is considered to be the sum of I_1 and I_4. This procedure yields the following expression for R_2

$$R_2 = \frac{\int'}{\varepsilon' + \mu'/R_3} \tag{12-13}$$

where $$\int' = V_{\text{OFF}} - V_{BE(\text{ON})} - \frac{2.5}{h_{FE}} \frac{(V_{CC} - V_{\text{ON}})(V_{\text{OFF}} - V_{BE(\text{ON})})}{V_{CC} - V_{\text{OFF}}}$$

$$\varepsilon' = \frac{2.5}{h_{FE}} \left[\frac{(V_{CC} - V_{\text{ON}})(I_2 + I_{CES})}{V_{CC} - V_{\text{OFF}}} + I_1 \right]$$

$$\mu' = V_{BE(\text{ON})}$$

and I_{CES} is collector reverse-leakage current of an OFF-state transistor.

Relative values of R_2 and R_3, together with V_{ON} of the flip-flop, determine $V_{BE(\text{OFF})}$ of the OFF-state transistor. If R_3 were infinitely large, $V_{BE(\text{OFF})}$ would be equal to V_{ON}. Since V_{ON} is generally less than the voltage required for significant forward bias of the base-emitter junction of a transistor, the flip-flop should function for large values of R_3. The actual value of R_3 is often determined by transient response of the flip-flop. As R_3 is made smaller, forward base drive is

reduced, and reverse base drive is increased. Where speed of operation is not important, a useful rule of thumb is to select R_3 such that

$$\frac{V_{ON}R_3}{R_2 + R_3} \leqslant 0.5V_T \tag{12-14}$$

where V_T is a turn-on threshold for the particular transistor used. Values of V_T for the germanium and the silicon transistor are approximately 0.15 and 0.5 volt, respectively, at room temperature. Satisfaction of the above inequality assures that base voltage to the OFF transistor is not greater than one-half the value required to turn on the device.

The value of R_1 is determined by substituting I_{CES} into Eq. (12-1); this yields

$$R_1 = \frac{V_{CC} - V_{OFF}}{I_2 + I_{B1} + I_3 + I_{CES}} \tag{12-15}$$

Equation (12-6) is used to determine $I_{B1} + I_3$ in the last expression; this permits the calculation of R_1.

12-9. DESIGNING THE TRIGGER FLIP-FLOP

Because the trigger flip-flop of Fig. 12-16 contains the various resistors of the basic flip-flop, the discussion of Sec. 12-8 is applicable to a dc design of the trigger stage. However, selection of resistors R_7 and R_8 in Fig. 12-16 is not included in the previous section. These resistors are generally in the neighborhood of 10 kilohms, although their exact values are not critical. The range of allowable values for these resistors is determined experimentally; too low a value will cause excessive loading at the R and S terminals, and too large a value will slow transient response of the stage.

Capacitance values required for the trigger flip-flop are dependent upon the choice of current and voltage levels, although general guidelines can be given for the particular transistor type used. The present circuit is symmetrical, so that $C_1 = C_2$ and $C_3 = C_4$. As a rule, the capacitances must be larger for the "slower" transistors than for the higher-speed devices. Table 12-4 gives typical capacitance values for three types of switching transistors.

Recovery time of the diodes is of importance for high-frequency operation of the trigger stage. Fast-recovery diodes should be used for input pulse-repetition rates above 200 or 300 khz.

Table 12-4. Typical Capacitance Values for Trigger Flip-flop Implemented with Various Types of Switching Transistors

Transistor type	C_1, C_2, pf	C_3, C_4
Alloy-junction	100	0.001 μf
Mesa or planar:		
Nonepitaxial	20	75 pf
Epitaxial	10	50 pf

12-10. OTHER TYPES OF COMPLEMENTING FLIP-FLOPS

A temporary memory, similar to that afforded by the input capacitors in Fig. 12-16, can be obtained by various methods. Several techniques exist in which gating circuitry is utilized to steer an input trigger signal to one or the other of two cross-coupled inverters. Pulse widths are controlled so that a set or reset signal is present only long enough to change the state of the flip-flop. Upon reaching its new state, the flip-flop receives no set or reset signal and remains at a stable condition until a second trigger signal is applied.

Consider the circuit in Fig. 12-21. A trigger pulse is applied to the common input line of two AND gates. The output lines of these gates serve as set and reset inputs to the cross-coupled inverters. One input line to each AND gate is connected to the output of the inverter which the gate drives. Assume that $\bar{P}$ is at a positive level. The positive-level trigger pulse is gated by A_1 and becomes the set input to the flip-flop; the circuit changes state, and P becomes positive. It is important that the trigger signal no longer be present after the circuit has changed state; otherwise, a reset pulse would be generated, and the stage would revert to its previous state. Hence, width of the trigger pulse must be less than transition time of the flip-flop. The circuit is reset to its original state upon application of a second trigger pulse.

Width of the trigger pulse may be controlled by either of the circuits shown in Fig. 12-22. The input signal and its inverse are applied to an AND gate in Fig. 12-22*a*. Turn-on delay of the inverter allows a slight overlap in the positive-level gate-input signals. This overlap allows a narrow trigger signal to be generated, as shown by the associated waveforms. The monostable multivibrator, or one-shot, is used to generate a narrow trigger pulse in Fig. 12-22*b*. Width of the trigger pulse is dependent upon component values and is not affected by duration of the input pulse.*

Circuits to control width of the trigger pulse may be external to the flip-flop, or they may be integral with the flip-flop and considered as part of it. This latter condition exists in many types of integrated-circuit flip-flops. The user is not concerned with applying a trigger pulse having a specified maximum width, as the necessary pulse-shaping circuitry is included within the integrated-circuit package.

A novel technique of steering a turn-on signal to the base of an OFF transistor utilizes a charge-storage effect in the collector-base diode of a transistor.[4] This

* A detailed discussion of the one-shot is given in Sec. 14-1.

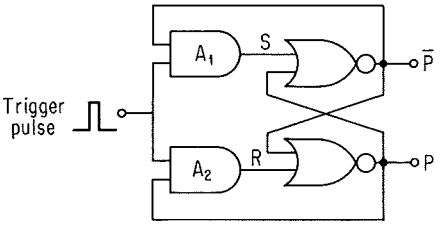

Fig. 12-21. Complementing flip-flop in which trigger pulse is gated by output state of flip-flop.

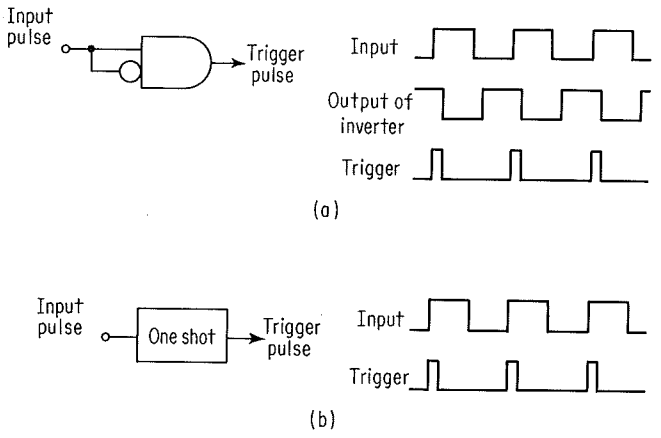

Fig. 12-22. Circuits to provide narrow trigger pulses. *(a)* **Turn-on delay of inverter provides pulse overlap to inputs of AND gate;** *(b)* **one-shot gives controlled-width trigger pulse.**

principle is illustrated in Fig. 12-23. Transistors Q_4 and Q_5 are cross-coupled in a flip-flop configuration. Consider that Q_4 is on, Q_5 is off, and the trigger pulse is at the $+V$ level. The relatively positive output-voltage level of Q_5 causes the output-voltage level of NOR gate 2 to be near ground potential; transistor Q_3 receives no base drive at this time. Both input lines to NOR gate 1 are close to ground potential; the relatively positive output-voltage level of this gate provides forward base current to transistor Q_2. As voltage at point A is at ground potential, base current of Q_2 flows out of the collector terminal of this device. Hence, a charge is stored in the collector-base diode of Q_2.

Let the trigger signal now fall to ground potential. Voltage at point A rises to a positive level, and the collector-base junction of Q_2 becomes reverse biased.

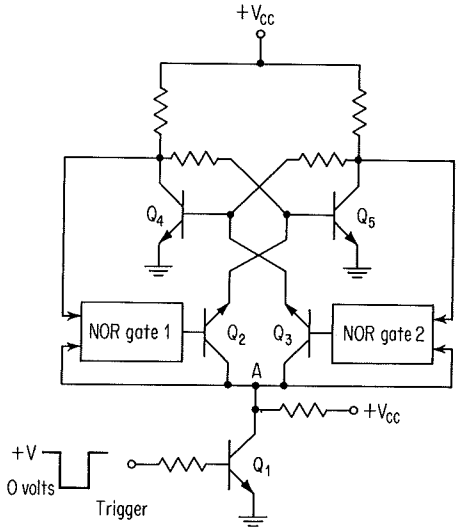

Fig. 12-23. Trigger flip-flop which utilizes charge-storage transistors.

The charge which was stored in Q_2 now flows out of the emitter of this device and turns on Q_5. At the same time, the positive level at A causes the output signal of each NOR gate to be near ground potential. This prevents any further current flow in either Q_2 or Q_3. When the trigger signal next rises to the $+V$ level, charge is stored in Q_3; this device turns on Q_4 when the trigger signal again falls to ground potential.

Pulse-width control is exercised in the above flip-flop stage. This is accomplished by the NOR gates, which permit only a momentary flow of emitter current in Q_2 or Q_3 (to remove stored charge and thus change the state of the flip-flop).

12-11. COMPLEMENTARY FLIP-FLOP

For all flip-flop circuits described to this point, two conflicting circuit requirements must be considered in selection of the collector load resistor. Consider the stage of Fig. 12-20 as an example. Ideally, collector load resistor R_1 should be a low resistance so that current I_2 to an external load can be at a high level. However, as R_1 becomes smaller, collector current increases in the saturated transistor. The value selected for R_1 is generally the maximum resistance which will permit the I_2 magnitude for a given V_{OFF} level. Whatever the value of R_1, this resistor provides a path for collector-current flow to the saturated transistor. ON-state collector current serves no useful purpose and merely increases power dissipation of the stage.

A circuit which eliminates excessive collector current of the saturated transistor is shown in Fig. 12-24.[5] The two pairs of complementary transistors are interconnected in a symmetrical fashion such that under steady-state conditions, either transistors Q_1 and Q_4 or Q_2 and Q_3 are in saturation. Consider that Q_1 is saturated; voltage at terminal $\bar{P}$ is equal to $V_{CC} - V_{CE(sat)}$. A voltage difference of $V_{CE(sat)}$ volts appears across the base-emitter junction of Q_3; consequently, this device is not turned on. The highly positive voltage level at $\bar{P}$ provides adequate forward base drive to Q_4, and this latter device is saturated. Forward base current of Q_1 flows into the collector of Q_4. A similar analysis to the above shows that a second stable state exists when Q_2 and Q_3 are saturated.

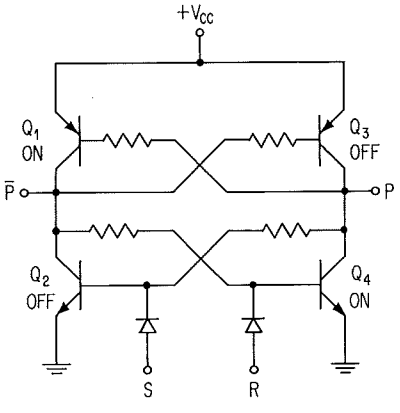

Fig. 12-24. Complementary flip-flop.

Except for negligible leakage currents, collector current of a saturated transistor consists solely of the base current required to turn on the diagonally opposite device. Because this base current is generally small, the circuit may have an extremely small power dissipation.[6]

Another outstanding feature of the present circuit is that relatively large load currents may be sinked or sourced at the output terminals. When current is *sinked* by a saturated N-P-N transistor, the flip-flop circuit itself makes only a small contribution to total collector current of the device. Consequently, larger currents can be sinked than with previous flip-flop designs. A saturated P-N-P transistor is able to *source* a considerable load current at nearly the $+V_{CC}$ level. This is in contrast to the current-limiting action imposed by a collector load resistor.

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13

Registers, Counters, and Diode Decoders

13-1. FLIP-FLOP AS A REGISTER ELEMENT

Flip-flops may be used in various circuit configurations to store binary information. When utilized for this purpose, the entire circuit is regarded as a *register,* with the individual flip-flop stages considered to be register elements.

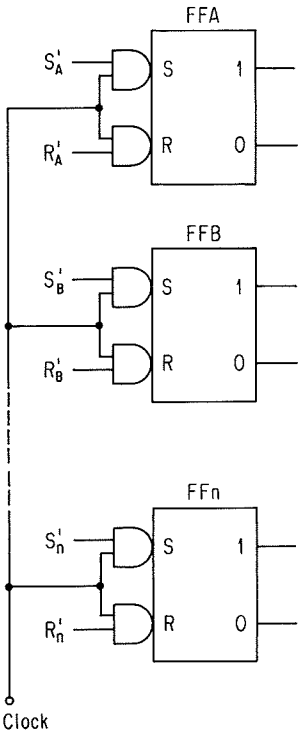

Fig. 13-1. Clocked *SR* flip-flops connected as a parallel register.

A block diagram of a *parallel* register is shown in Fig. 13-1. Each flip-flop is a clocked *SR* type described in Sec. 12-3. When the clock pulse is at a positive level, information appearing at the S' and R' terminals of each stage determines whether a 1 or a 0 is to be stored in that stage. The stored information is retained until the next positive clock-pulse signal appears. This allows the register to continue to store information even though the input information may no longer be present.

As an example of another form of parallel register, each R' terminal in the above figure may be connected to a common reset line, with binary information applied only to the S' terminal of each stage. Operation is such that a reset pulse is applied to clear all flip-flops to the 0 state. The clock signal is then applied; each flip-flop having a 1 input at its S' terminal is set to the 1 state at this time.

Figure 13-2 shows the clocked *SR* flip-flop connected as a serial, or shift, register. Each time the clock-pulse signal becomes positive, a 1 or a 0 is transferred into *FFA.** At the same time, information stored in each flip-flop is *shifted* into the next succeeding stage.

The clock-pulse signal to the above circuit must have a minimum width in order to gate input informa-

* This notation is used to denote flip-flop *A*, etc.

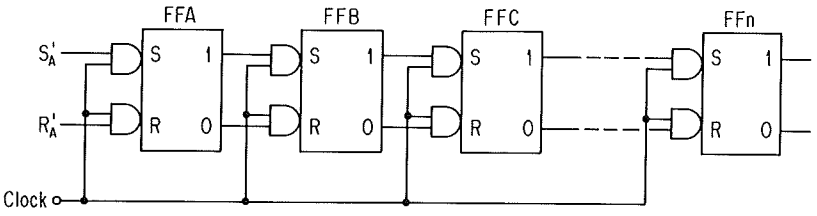

Fig. 13-2. Clocked *SR* flip-flops connected as a serial, or shift, register.

tion into a stage. However, if width of the clock pulse is greater than propagation time of a flip-flop, the bit which was stored in *FFA* would be transferred to *FFB*, and so on. This would constitute a *race* condition, which would make the circuit useless. Because of the stringent requirement upon width of the clock pulse, the shift-register configuration shown above is not widely used.

A shift-register configuration which alleviates the problem of maintaining careful control over width of a clock pulse is shown in Fig. 13-3. Two alternate clock pulses, ϕ_1 and ϕ_2, are used to transfer information from one stage to the other. This is illustrated by the timing diagram of Fig. 13-4. It is assumed that each flip-flop is initially at the 0 state and that the S'_A input is positive. When ϕ_1 becomes positive at time t_0, output A rises to a positive level. A 1 signal is now applied to the set terminal of stage B; consequently, when ϕ_2 becomes positive at time t_1, output B rises to a positive level. The 1 which had previously been stored in *FFA* has now been shifted into *FFB*. An extension of this analysis shows that ϕ_1 and ϕ_2 transfer information into flip-flops C and D, respectively. Care must be taken to assure that the ϕ_1 and ϕ_2 pulses do not overlap to the extent that a race condition can occur.

This last shift register utilizes two flip-flops per bit, whereas only one flip-flop per bit is required for the shift register of Fig. 13-2. The addition of one flip-flop was necessary to prevent a race condition. When two flip-flops are used to store one bit, the input and output flip-flops are often referred to as "master" and "slave," respectively. In the circuit of Fig. 13-3, information is transferred into a master flip-flop by ϕ_1 and into a slave flip-flop by ϕ_2.

It is common practice to regard a pair of master-slave flip-flops as a single flip-flop. This is often the case with integrated-circuit configurations, where the ϕ_2 pulse is generated internally. Insofar as the external-circuit connections are con-

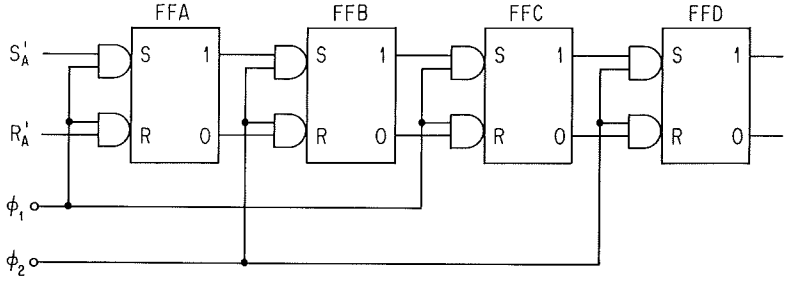

Fig. 13-3. Shift-register configuration to eliminate race condition.

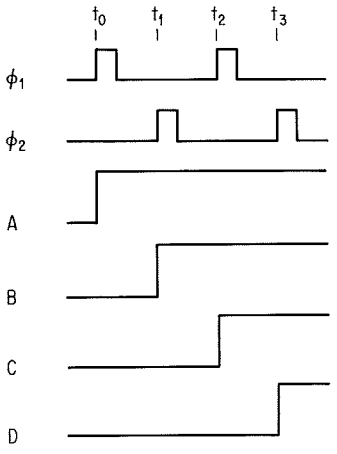

Fig. 13-4. Timing diagram for shift register of Fig. 13-3; each flip-flop is initially at the 0 state, and S_A is positive.

cerned, only a single pair of set and reset lines, a single clock-pulse line, and a single pair of output lines are brought out of the header.

Trigger flip-flops may also be used to implement the shift register. When this is done, only a single clock pulse and a single flip-flop per bit are required. Consider the circuit of Fig. 12-16 in this application. Let this stage be connected in the shift-register configuration of Fig. 13-5. Inputs S_A and R_A are complementary; one input is at 1 while the other is at 0. Similarly, all remaining flip-flops have complementary input signals. When the clock-pulse signal is at a positive level, the binary 1 set or reset input level to each stage determines which of the input steering capacitors is charged. As the clock signal falls to ground potential, the information stored in a stage is transferred to the next stage. The delay afforded by the steering capacitors prevents any race condition.

13-2. COUNTING WITH SHIFT REGISTERS

A simple form of counter is shown in Fig. 13-6. Flip-flop stages are connected in a shift-register configuration, with the output of the nth stage connected to the input of the first stage. Each flip-flop may be implemented with a single trigger flip-flop or with a master-slave pair of flip-flops. If the latter circuit arrangement is employed, a second clock signal may be added externally, or it may be generated internally. The following analysis treats the circuit as a shift register containing only a single flip-flop per bit and having a single clock-pulse input signal; this analysis applies regardless of the specific flip-flop arrangement.

Preset and clear input terminals are shown in Fig. 13-6. A positive signal to the preset line sets the flip-flop to 1, and a positive signal to the clear line resets, or clears, the flip-flop to 0. The preset and clear inputs are *direct,* i.e., the input pulse is not gated by any clock or trigger signal. This can be accomplished, for instance, by connecting the input signal to a base-input diode, as shown in Fig. 12-5, or to a pullover transistor, as shown in Fig. 12-11.

Operation of the above circuit is as follows. Before applying the clock pulse, a single start pulse is applied; this sets the first stage to 1 and the remaining stages

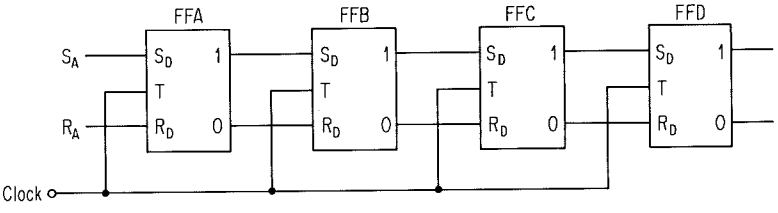

Fig. 13-5. Shift register implemented with trigger flip-flops.

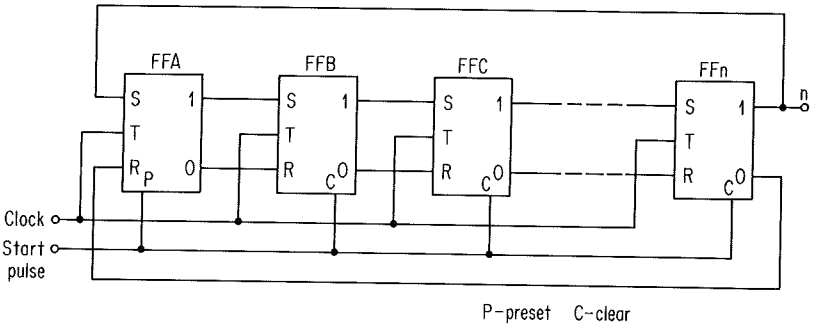

Fig. 13-6. Shift register connected as a ring counter.

to 0. The 1 stored in the first flip-flop is shifted one stage to the right by each succeeding clock pulse. (The actual shift may occur during the leading or trailing edge of the clock pulse; this is determined by the particular type of flip-flop used.) Figure 13-7 shows waveforms for several cycles of clock signal.

Feedback from the *n*th stage to the first stage causes the stored 1 to be shifted in a ring fashion around the entire register. For this reason, the circuit is often referred to as a "ring counter."[1] The stored 1 appears in sequence at each true-output line and reappears at any given line after every *n* pulses. Consequently, the circuit counts to the number *n* (where *n* is the number of individual stages).

Another form of *n*-stage feedback shift register counts in sequential fashion to the number 2*n*. This is accomplished by cross-coupling the output of the last stage to the input terminals of the first stage.[2,*] Figure 13-8 shows five flip-flops, *FFA* to *FFE*, connected for this type of operation; the circuit is often referred to as a "Johnson counter." The *inverse* of the signal stored in *FFE* is transferred into *FFA* each time a shift of information occurs. Consider that all flip-flops are initially at the 0 state. The first clock pulse transfers a 1 into *FFA* and a 0 into all remaining stages. For the next four clock pulses, ones are fed back from *FFE* to *FFA*. Hence, after five clock pulses, the register is filled with ones. At this time, a 0 is fed back to *FFA*; the sixth to tenth clock pulses store zeros in *FFA*. After the tenth pulse, each flip-flop stores a 0, and the above cycle is repeated. The register

* This circuit configuration is one form of a more general class of feedback shift registers. The general class of feedback shift registers is described in Sec. 13-8.

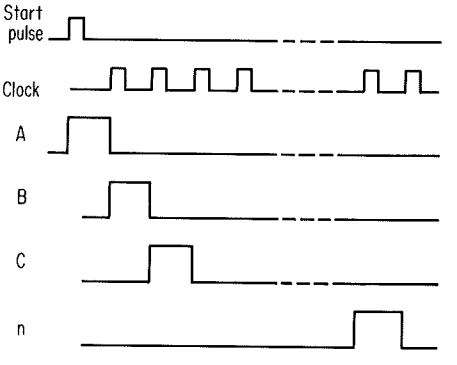

Fig. 13-7. Waveforms for ring counter of Fig. 13-6.

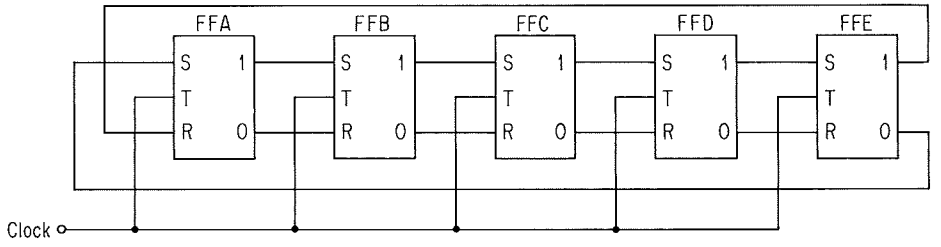

Fig. 13-8. Shift register connected to recycle after 10 input pulses.

is seen to fill alternately with ones and with zeros. Table 13-1 shows the above sequence; input pulses are numbered 0 to 10. The table shows that 10 input pulses are required to advance the counter to its original state.

There are 32 possible combinations for the output states of five flip-flops. Hence, when power is initially applied to the register of Fig. 13-8, the sequence of stored bits may not correspond to any of the 10 states listed in Table 13-1. The sequence of bits initially stored in the register will repeat itself at intervals of 10 clock pulses. However, unless the register cycles through a *known* sequence, it is not possible to determine which decimal count is stored in the register.

A reset pulse can be applied to all registers before beginning a count. This brings all stages to the sequence corresponding to decimal number 0 (or 10) in Table 13-1.

The register can be *forced* to a desired combination of ones and zeros by using logic in the feedback path. Figure 13-9 shows two circuits which force the register to one of the 10 sequences listed in Table 13-1.[3,4] For either circuit, the particular forced sequence is dependent upon which sequence was initially stored in the register. Upon reaching the forced sequence, the register then cycles through the various sequences shown in the table.

Figure 13-9*a* shows a feedback technique which can be used when the register is implemented with NOR-type set-reset flip-flops, i.e., the individual stages are of the master-slave variety. A 1 is cross-coupled to the reset input of *FFA* only when the true outputs of *FFD* and *FFE* are at the 1 state (to give $DE = 1$). Inspection of Table 13-1 shows that this occurs when input pulses 5, 6, 7, and 8 are stored in the register. For the condition where input pulse 9 is stored, feedback signals DE and $\bar{E}$ are both at the 0 state. Consequently, *FFA* remains in its present state (storing a 0) at the tenth input pulse. The feedback network can also be used with *JK* flip-flops. However, because both input signals to *FFA* can be at the 0 level simultaneously, this feedback network is not suitable when the register is implemented with the NAND-type set-reset flip-flop or with the trigger flip-flop of Fig. 12-6.

Table 13-1. Sequence Table for True Outputs of Johnson Counter

Input pulse (decimal number)	True outputs *A B C D E*
0	0 0 0 0 0
1	1 0 0 0 0
2	1 1 0 0 0
3	1 1 1 0 0
4	1 1 1 1 0
5	1 1 1 1 1
6	0 1 1 1 1
7	0 0 1 1 1
8	0 0 0 1 1
9	0 0 0 0 1
10	0 0 0 0 0

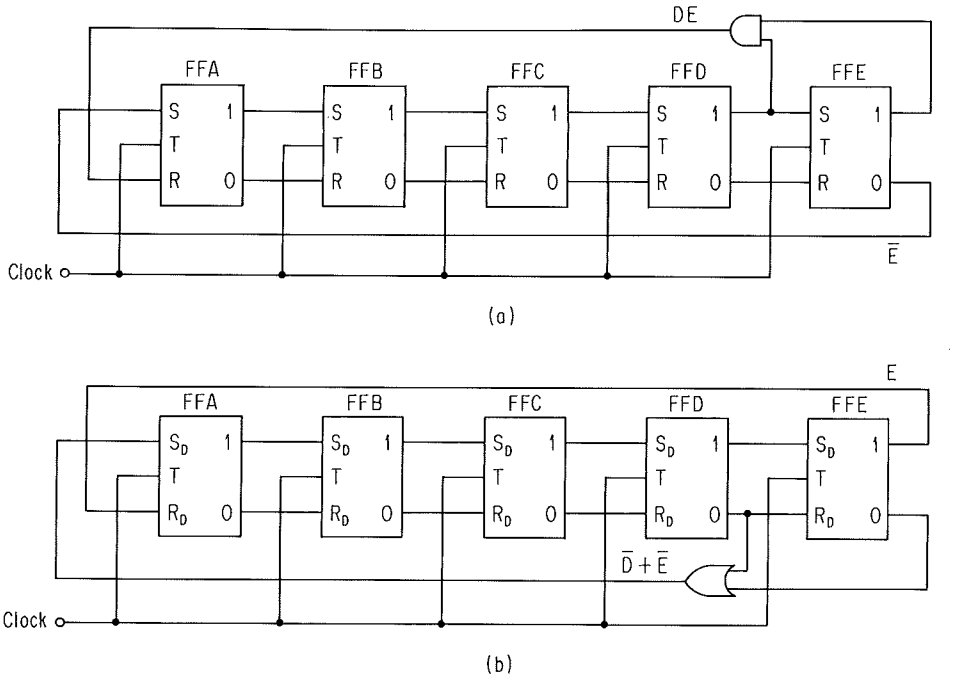

Fig. 13-9. Feedback logic which forces registers to cycle through in a known sequence. *(a)* **Feedback suitable for master-slave flip-flop;** *(b)* **feedback suitable for trigger flip-flop.**

The circuit shown in 13-9*b* is suitable for use with the above trigger flip-flop and with the NAND-type set-reset flip-flop. The feedback logic prevents both the set and reset inputs to *FFA* from being at the 0 level simultaneously. Hence, there can be no ambiguous operation of *FFA*. This feedback arrangement is not suitable for use with NOR-type set-reset flip-flops, nor can it be used with *JK* flip-flops.

Although the above counter has 10 distinct states, the method of detecting the stored decimal number is different from that used with the ring counter of Fig. 13-6. This is because any single stage in the feedback shift register has a true output consisting of alternate sequences of five ones and five zeros. The decimal number stored within the register at any given time is obtained by decoding the output state of the individual flip-flop stages. A diode-resistor network to perform this function is described in the following section.

13-3. DECODING FOR DECIMAL OUTPUTS

A decode gate is a network having two or more input signals and a single output signal; the output signal is present only when all input signals are at a prescribed binary level. The diode AND gate described in Sec. 10-2 is an example of a decode gate. A two-input diode AND gate is shown in Fig. 13-10. This circuit has a positive-

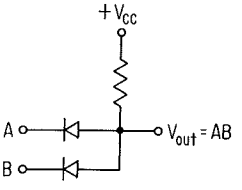

Fig. 13-10. Two-diode AND gate.

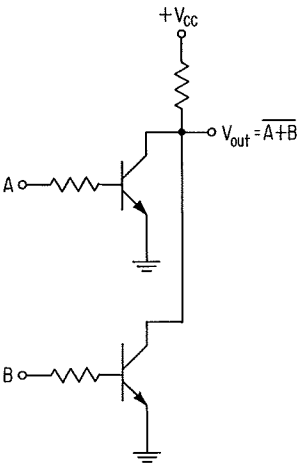

Fig. 13-11. Two-transistor decode gate.

output level only when both input signals are positive. Positive logic is used throughout this chapter; hence, the above decode gate has a 1 output when both inputs are 1.

Another form of decode gate is obtained by connecting two transistors as shown in Fig. 13-11. The circuit has a 1 output only when both inputs are 0. This form of decode gate has not been so popular as the diode AND gate. Consequently, the diode AND gate is alluded to in all further discussions of diode gates.

Two or more decode gates may be used in a system. When this is done, the group of decode gates is referred to as a "decoder." Hence, the decoder network may have several output lines. Generally, there are fewer output lines than input lines.

Table 13-1 shows that there is a unique five-variable combination of ones and zeros stored within the feedback shift register for each of the 10 input pulses. Hence, a separate logic expression can be written to show the state of each flip-flop. These logic expressions are shown in Table 13-2 for the corresponding decimal numbers.

As each of the logic expressions in Table 13-2 can be realized by means of a five-input diode AND gate, a decoder can be used to obtain each of the 10 decimal counts. The decoder will have 10 output lines, with each line corresponding to a separate decimal number from 0 to 9. Only one of these output lines will be energized at any given time.

The logic expressions presented in Table 13-2 are not in their simplest form. This is verified, for instance, by noting that the expression $\bar{A}\bar{E}$ is also unique for decimal number 0. The remaining decimal numbers can likewise be represented by two variables, instead of by the five variables given in the table. A technique for obtaining simplified expressions for the present counter, as well as for other types of counters, is described in the following section.

Table 13-2. Stored Decimal Numbers and Logic Expressions for Johnson Counter

Decimal number	Logic expression
0	$\bar{A}\bar{B}\bar{C}\bar{D}\bar{E}$
1	$A\bar{B}\bar{C}\bar{D}\bar{E}$
2	$AB\bar{C}\bar{D}\bar{E}$
3	$ABC\bar{D}\bar{E}$
4	$ABCD\bar{E}$
5	$ABCDE$
6	$\bar{A}BCDE$
7	$\bar{A}\bar{B}CDE$
8	$\bar{A}\bar{B}\bar{C}DE$
9	$\bar{A}\bar{B}\bar{C}\bar{D}E$

13-4. LOGIC SIMPLIFICATION WITH THE KARNAUGH MAP

Let us digress from the subject of counters and consider certain characteristics of Boolean functions. Any given Boolean expression may contain one or more variables or terms which could just as well be omitted; an expression of this nature is considered to exhibit redundancy. The function

$$f_1 = AB + ABC \qquad (13\text{-}1)$$

can be reduced to

$$f_1 = AB \tag{13-2}$$

Hence, the term ABC in Eq. (13-1) is redundant.

An expression may contain no redundant variables or terms but still not be in the simplest form. For purposes of this discussion, a function is considered to be in the simplest form when a minimum number of diodes is required to implement the logic circuit. The two expressions

$$f_2 = \bar{A}\bar{C}\bar{D} + B\bar{C}\bar{D} + ABD + BCD \tag{13-3}$$

$$f_3 = \bar{A}\bar{C}\bar{D} + AB\bar{C} + BCD \tag{13-4}$$

have the same truth table and are thus logically equivalent to each other. Equation (13-3) is implemented with 16 diodes, whereas only 12 diodes are required to implement Eq. (13-4). Because it is not possible to reduce Eq. (13-3) to an expression which requires fewer than 12 diodes, Eq. (13-4) is considered to be a minimal form of the function given in Eq. (13-3).

Several methods exist for the minimization of Boolean expressions.[5-7] One of these methods, utilizing a Karnaugh map, is described below. The following discussion does not present an extensive treatment of Karnaugh map analysis; rather, the intent is to point out certain features of this simplification method. More detailed descriptions of this form of analysis are presented in the literature.*

A Karnaugh map consists of a rectangle divided into squares, referred to as "cubes," or "cells." The variables of a function are listed on two sides of a rectangle; all combinations of 0 and 1 are assigned to the variables. Figure 13-12*a* illustrates a Karnaugh map rectangle for the variables A and B. For purposes of further discussion, the cubes are labeled C_1 to C_4.

A Boolean function is *mapped* into the above rectangle in the following manner. All possible values of the variable are substituted into the expression. Each resulting 1 is placed in those cubes which are responsible for the 1; a 0 is placed in all remaining cubes. For instance, consider the function

$$f = AB \tag{13-5}$$

This expression yields 1 only for $A = 1$ and $B = 1$. Hence, a 1 is placed in C_4 and a 0 is placed in the remaining cubes; this is shown in Fig. 13-12*b*. Figure 13-12*c* and *d* shows mappings of the functions

$$g = \bar{A} + B \tag{13-6}$$

$$h = A\bar{B} \tag{13-7}$$

* Excellent treatments of this subject are given in Refs. 6 and 7.

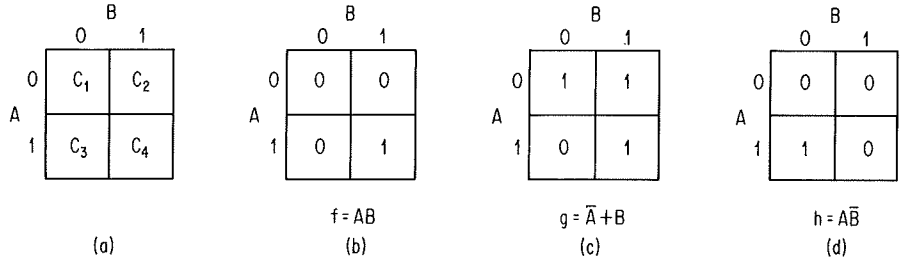

Fig. 13-12. Karnaugh map for functions of two variables.

The Karnaugh map allows many complex Boolean expressions to be simplified in a systematic manner. In addition, the map is useful in synthesizing expressions. By following certain elementary rules, the resulting functions are nonredundant and minimal. Because of the ease with which two- and three-variable expressions can be algebraically manipulated, the Karnaugh map is most often used for expressions containing four or more variables.

Figure 13-13*a* shows a map to represent four variables. The map is a 4 by 4 rectangle containing all possible combinations of the terms A, B, C, and D. Figure 13-13*b* shows a mapping for the function

$$f = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}BCD + AB\bar{C}\bar{D} + ABCD \tag{13-8}$$

Looking at the first term, $\bar{A}\bar{B}\bar{C}\bar{D}$, in the above expression, we see that it is 1 when all variables are 0; consequently, a 1 is placed in cube C_1. The remaining terms are mapped in a similar manner.

Adjacent cubes in the above Karnaugh map differ by only one variable. A cube along the *left* edge of the map differs by only one variable from the cube in the same row along the *right* edge of the map. Similarly, a cube along the *top* edge of the map and the cube in the same column along the *lower* edge of the map differ by only one variable. Any two cubes which differ in only one variable from each other are considered to be *adjacent* cubes. Hence, the Karnaugh map exhibits end-around adjacency.

If two adjacent cubes contain a 1, the variable which is *not* common to the two cubes can be eliminated from the Boolean expression for the two cubes. This is illustrated, for instance, by considering cubes C_{10} and C_{11} in the four-variable map. An expression for these two cubes is written

$$g = AB\bar{C}D + ABCD \tag{13-9}$$

The product ABD can be factored out of the above expression to yield

$$g = ABD(\bar{C} + C) \tag{13-10}$$

It can be shown that

$$\bar{C} + C = 1 \tag{13-11}$$

Hence, Eq. (13-10) can be simplified to

$$g = ABD \tag{13-12}$$

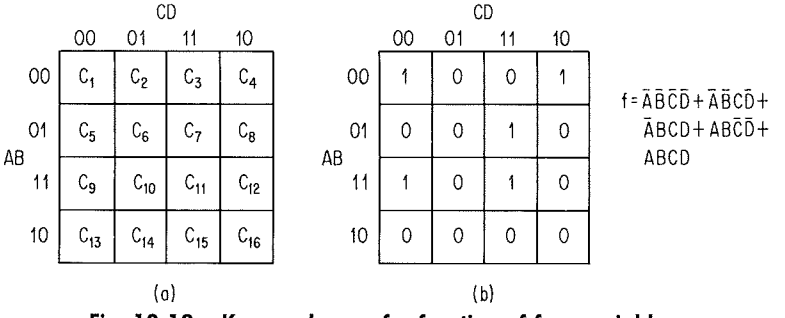

Fig. 13-13. Karnaugh map for function of four variables.

This shows that the two adjacent cubes can be represented by only three variables instead of by four variables. A similar analysis applies to all adjacent cubes within the four-variable Karnaugh map.

A grouping of one or more adjacent cubes which contain 1 is referred to as a "subcube." All cubes within a subcube are often looped to indicate the particular grouping chosen. Figure 13-14 shows the Karnaugh-map plot of Eq. (13-8), together with three indicated subcubes. The two open loops on the top row are considered to be connected. An expression to represent the three subcubes can be written

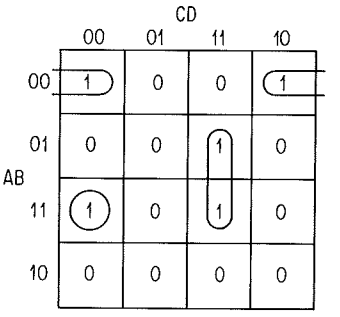

Fig. 13-14. Karnaugh map plot of Eq. (13-8).

$$h = \bar{A}\bar{B}\bar{D} + AB\bar{C}\bar{D} + BCD \qquad (13\text{-}13)$$

This last expression, which is a simplified form for Eq. (13-8), contains no redundant terms and also is a minimal form of the function.

Subcubes in the four-variable Karnaugh map may contain one, two, four, or eight cubes. As shown above, there is one less variable in the simplified Boolean expression for a two-cube, or two-cell, subcube than in the original expression for either of the two cubes. Similarly, the four- and eight-cell subcubes permit reductions of two and three variables, respectively.

It often happens that the same mapped function may be segregated into different numbers of subcubes, depending upon the size chosen for each subcube. This can lead to a simplified function which contains at least one redundant term. A procedure for preventing this is to loop all ones which will make the smallest subgroup and which will not combine into the next larger subgroup. This procedure is followed until all ones have been looped.[7]

By following the above rule for subdividing a Karnaugh map into subcubes, the logic designer is assured of a Boolean expression which contains no redundant terms. However, in some instances, this technique alone does not assure that the resulting expression is a minimal form of the function. An uncertainty arises when the Karnaugh map is divided, by the above rule, into more subcubes than is absolutely necessary. In order to assure a minimal form of the function, the Karnaugh map analysis can be applied to obtain all possible nonredundant solutions. Inspection of the resulting solutions will show which are minimal forms of the function.

Boolean expressions containing five variables may also be plotted on the Karnaugh map. One widely used topology is shown in Fig. 13-15. This particular map utilizes eight rows and four columns to represent all combinations of the five variables. Each cube differs in only one variable from an adjacent cube. However, there are also cubes in nonadjacent rows which differ from each other by only one variable. Figure 13-15 indicates those rows which do differ by only one variable; this is shown by placing crosses in the columns and connecting appropriate rows by a vertical line. Each pair of connected crosses indicates two rows which differ by only one variable.

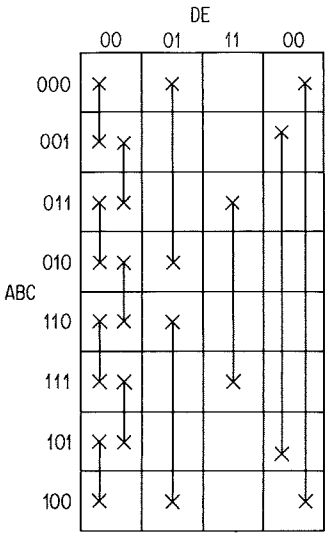

Fig. 13-15. Karnaugh map for functions of five variables; connected crosses show rows which differ by only one variable.

ABC \ DE	00	01	11	10
000	0	9	8	θ
001	θ	θ	7	θ
011	θ	θ	6	θ
010	θ	θ	θ	θ
110	2	θ	θ	θ
111	3	θ	5	4
101	θ	θ	θ	θ
100	1	θ	θ	θ

Fig. 13-16. Karnaugh map plot of decimal numbers given in Table 13-2.

At this point, another aspect of logic reduction is introduced. In many circuit applications, there are certain combinations of variables which will not occur. For instance, the sequence $\bar{A}B\bar{C}DE$ does not occur in Table 13-1. Consequently, either a 1 or a 0 may be placed in the cube representing the above sequence on a Karnaugh map. In order to show that the cube may represent either a 1 or a 0, the symbol θ is used throughout this chapter. A cube which contains a θ represents an "optional term."*

It is now possible to simplify the Boolean expressions for the Johnson counter described in Sec. 13-2. The decimal numbers 0 to 9 are located on the Karnaugh map according to their logic expressions given in Table 13-2. Figure 13-16 shows the Karnaugh map representation for each decimal number. The presence of a decimal number within a cube indicates that a binary 1 is stored within that cube.

The above map has 22 cubes which do not contain a decimal number. Ordinarily, these cubes would be filled with 0s. However, as the register is constrained to store only those sequences already mapped, the remaining 22 cubes are shown to contain optional terms. This use of optional terms permits considerable simplification of the Karnaugh map plot.

There are 10 *separate* Boolean expressions represented in Fig. 13-16. Hence, it is not permissible to combine the decimal numbers into subcubes. However, a decimal number and an optional term can be combined into a subcube when they are adjacent on the same row or when they exhibit the vertical adjacency shown in Fig. 13-15. Each of the ten decimal numbers can be combined with

*This optional term is often referred to as a "don't care" term. However, because one does care whether or not a term occurs, "optional" is used here.

seven optional terms; this yields eight-cell subcubes, thus permitting a reduction of three variables for each expression. Hence, each of the 10 decimal numbers can be decoded by a separate two-input AND gate. Table 13-3 gives the simplified logic expression for each of the 10 decimal numbers.

Table 13-3. Decimal Numbers and Simplified Logic Expressions for Johnson Counter

Decimal number	Simplified logic expression
0	$\bar{A}\bar{E}$
1	$A\bar{B}$
2	$B\bar{C}$
3	$C\bar{D}$
4	$D\bar{E}$
5	AE
6	$\bar{A}B$
7	$\bar{B}C$
8	$\bar{C}D$
9	$\bar{D}E$

13-5. BINARY COUNTERS

Consider that the circuit of Fig. 12-16 is connected as a complementing flip-flop. Each time the input signal changes from 1 to 0, the flip-flop changes state. As the circuit has only two stable states, the output signal alternates between 1 and 0 for successive input pulses. Table 13-4 shows the sequence of output signals for four input pulses. The output signal is seen to repeat itself for every second input pulse.

Table 13-4. Sequence of Input and Output Signals for Complementing Flip-flop

Input signal	Output signal
0	0
1	1
2	0
3	1

Let four of the above complementing flip-flops be connected as shown in Fig. 13-17. Each time the input signal to a flip-flop changes from 1 to 0, the flip-flop switches state. The sequence of true output signals for this cascade arrangement of flip-flops is shown in Table 13-5. Sixteen input pulses (0 to 15) are shown in the table. It is clear that the circuit has been cycled through all combinations of 1 and 0 by the 16 input pulses. The circuit is thus capable of counting to 16.

Table 13-5. Sequence Table for True Outputs of Flip-flops in Fig. 13-17

Input pulse	*A B C D*
0	0 0 0 0
1	1 0 0 0
2	0 1 0 0
3	1 1 0 0
4	0 0 1 0
5	1 0 1 0
6	0 1 1 0
7	1 1 1 0
8	0 0 0 1
9	1 0 0 1
10	0 1 0 1
11	1 1 0 1
12	0 0 1 1
13	1 0 1 1
14	0 1 1 1
15	1 1 1 1

Any complementing flip-flop can be cascaded to generate the above table of ones and zeros. Instead of switching during the 1 to 0 transition at the input, certain types of flip-flops switch state each time the input signal changes from 0 to 1. If flip-flops having this latter characteristic are used, the *complementary* output of a flip-flop is used to drive a succeeding stage.

The left-to-right counting sequence of Table 13-5 is identical to the right-to-left counting sequence of Table 9-1. This latter table was shown to represent the decimal numbers 0 to 15 in binary notation. Con-

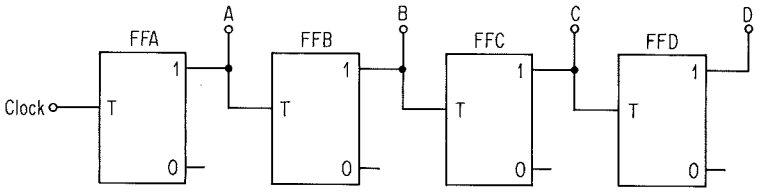

Fig. 13-17. Cascade connection of complementing flip-flops.

sequently, the various bit positions in Table 13-5 can be interpreted, from left to right, as representing ascending powers of 2. Hence, *FFA* stores 2^0, *FFB* stores 2^1, etc. The cascade connection of complementing flip-flops counts in binary fashion and is referred to as a *binary* counter; an n-stage binary counter counts to the number 2^n. For any binary counter, the decimal number stored is identical to the number of input pulses (up to the number 2^n, at which time the counter recycles).

Decoding of the binary counter is accomplished with diode AND gates. A logic expression for each decode gate of the four-stage counter can be written directly from Table 13-5. The Karnaugh map could be used to plot the 16 Boolean functions. However, as a binary counter cycles through *each* of 2^n states, each cube of the map would contain a decimal number. Consequently, it is not possible to simplify the original expressions. This statement applies, regardless of the size of a binary counter. However, as shown in the following section, the decode logic can often be implemented in two or more steps, thus reducing the *total* number of diodes. Table 13-6 shows the stored decimal numbers and corresponding logic expressions for the four-stage binary counter of Fig. 13-17.

Let us now investigate the manner in which a 1 is propagated through the

Table 13-6. Stored Decimal Numbers and Logic Expressions for Four-stage Binary Counter

Decimal number	Logic expression
0	$\bar{A}\bar{B}\bar{C}\bar{D}$
1	$A\bar{B}\bar{C}\bar{D}$
2	$\bar{A}B\bar{C}\bar{D}$
3	$AB\bar{C}\bar{D}$
4	$\bar{A}\bar{B}C\bar{D}$
5	$A\bar{B}C\bar{D}$
6	$\bar{A}BC\bar{D}$
7	$ABC\bar{D}$
8	$\bar{A}\bar{B}\bar{C}D$
9	$A\bar{B}\bar{C}D$
10	$\bar{A}B\bar{C}D$
11	$AB\bar{C}D$
12	$\bar{A}\bar{B}CD$
13	$A\bar{B}CD$
14	$\bar{A}BCD$
15	$ABCD$

binary counter of Fig. 13-17. It is assumed that a flip-flop changes state each time the input signal changes from 1 to 0. Consider that a 1 is stored in each stage. When the clock signal to *FFA* falls toward ground potential, this stage switches to the 0 state; a negative-going signal appears at the true output of *FFA*. Consequently, *FFB* is triggered, and a negative-going signal is applied to *FFC*. This latter stage changes state and, in turn, causes *FFD* to switch to the 0 state. All stages have now switched to the 0 state, but not simultaneously. It was necessary for a negative-going signal to ripple through all stages. Hence, this circuit configuration is often referred to as a "ripple-through counter." The circuit is also regarded as a "sequential counter," because the trigger signal is propagated in sequence through each successive stage.

Figure 13-18 illustrates one cycle of clock signal, together with the true-output waveforms of *FFA* through *FFD*, for the propagation of a 1 through the above counter. The clock signal begins its fall toward 0 at time t_0, and each successive stage introduces a delay in the propagated 1; consequently, output *D* does not reach 0 until time t_x. Because of the additive delays, the decoded outputs from a sequential counter may not reach their final states until a significant time after the clock signal begins its negative-going transition. This delay in output response is not tolerable for many high-speed counting applications. In addition, as frequency of the clock signal is increased, there may be little or no overlap of waveforms which are to be decoded in the same AND gate.

The cumulative propagation delays described above can be eliminated by interconnecting the various flip-flops as shown in Fig. 13-19. The input to each stage beyond *FFA* consists of the ANDed combination of clock signal and the true output of *each* previous flip-flop. Examination of Table 13-5 reveals that a stage changes state only when all *previous* stages were at 1. Hence, when the clock signal to the circuit is positive, a 1 is applied to those stages which are to change state during the 1-to-0 transition of the clock signal; this permits charging of the appropriate input capacitors. During the negative-going edge of the clock signal, all inputs which were at 1 fall toward the 0 level. Consequently, a negative-going input signal is applied *simultaneously* to each of the stages to be triggered. All transitions are now completed during the propagation-delay time of a single stage.

This latter counter configuration is referred to as a "synchronous counter." Because of the necessity to AND together the true outputs of all previous stages, there are practical limits to the number of stages which may be cascaded in the above fashion. One method of restricting the number of diodes to a reasonable figure is to split the counter into two or more synchronous counters, with the final stage of

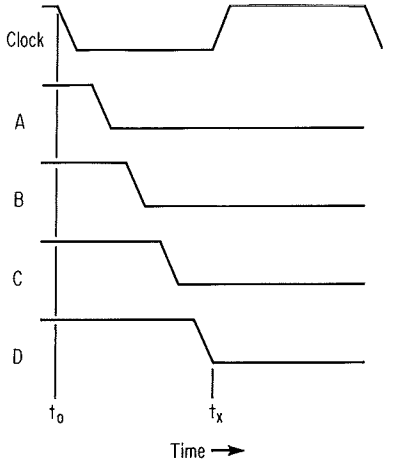

Fig. 13-18. Waveforms to illustrate effects of propagation delay in the counter of Fig. 13-17.

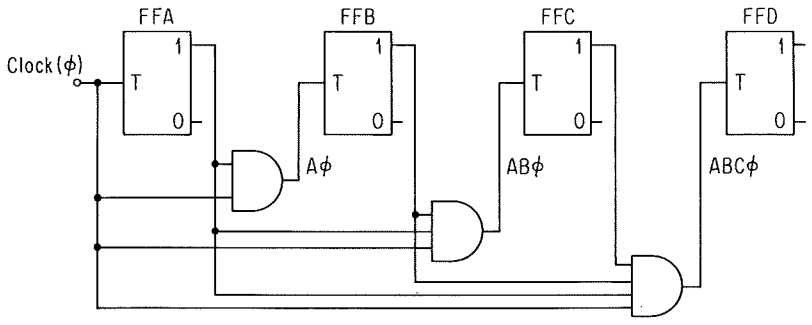

Fig. 13-19. Binary-counter configuration which minimizes effect of propagation delay.

one synchronous counter connected in sequential fashion to the first stage of the succeeding synchronous counter. The last output signal from a synchronous counter serves as the clock signal to all AND gates in the succeeding synchronous counter. This reduces loading of the original clock-pulse generator.

When synchronous counters are cascaded in the above fashion, the output waveforms of each successive synchronous counter are delayed with respect to the waveforms of the previous synchronous counter. If the number of cascaded synchronous counters becomes large, the same problem of propagation delay may be encountered as was observed for the sequential counter.

13-6. LARGE-SCALE DECODING

By performing a decoding operation in two steps, it is often possible to reduce the number of required diodes. The following discussion illustrates the manner in which this may be applied to the four-stage binary counter. The same principle of diode reduction applies, of course, to all decoders.

Inspection of the 16 AND functions in Table 13-6 reveals that any combination of two variables is repeated four times. For instance, the two-variable term $\bar{A}\bar{B}$ is contained in the expressions for decimal numbers 0, 4, 8, and 12. This two-variable term is ANDed with all possible AND combinations of C and D to form the four-variable function for each of the above decimal numbers. Likewise, all other AND combinations of A and B are ANDed with all AND combinations of C and D.

Instead of decoding each of the 16 decimal numbers in a separate four-input AND gate, decoding can be accomplished by obtaining all combinations of A and B, and combining *each* of these outputs with all combinations of C and D. Figure 13-20 illustrates this two-step manner of decoding. Four two-input AND gates provide combinations of A and B, and four two-input AND gates provide combinations of C and D. Each of the gate outputs containing A and B is ANDed with each of the gate outputs containing C and D. The total number of required diodes is obtained in the following manner:

1. Four two-input AND gates for combining A and B: $4 \times 2 = 8$ diodes.
2. Four two-input AND gates for C and D: $4 \times 2 = 8$ diodes.
3. Sixteen two-input AND gates for combining outputs of 1 and 2 above: $16 \times 2 = 32$ diodes.

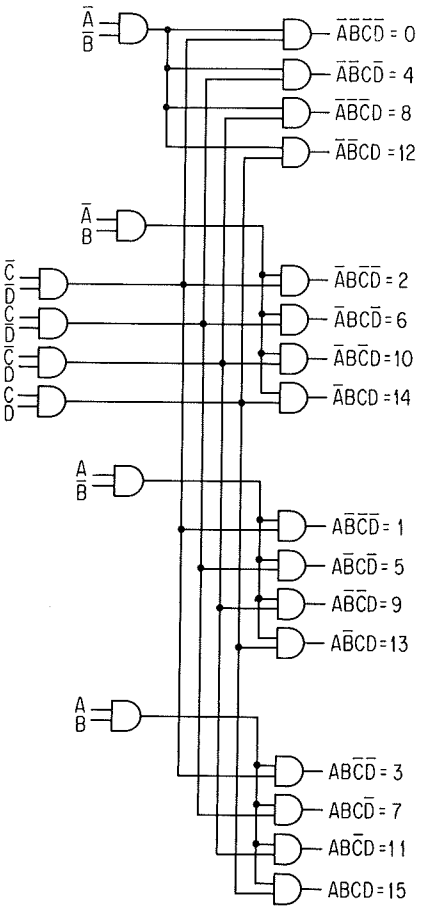

Fig. 13-20. Two-step decoding for four-stage binary counter.

Summation of the above numbers reveals that the two-step decoder is implemented with 48 diodes. From Table 13-6, decoding in one step requires 16 four-input AND gates for a total of 64 diodes. Hence, the two-step decoding technique provides a considerable reduction in the number of diodes.

Fan-out loading of a flip-flop is increased when decoding is performed in two steps. This is illustrated for the four-stage binary counter by considering loading effects of the single- and two-step decoders. Table 13-6 shows that each flip-flop output fans out to eight AND gates in the single-step decoder. Hence, current from eight AND gates flows into the output terminal of each flip-flop. However, a flip-flop output does not sink *total* current of all eight gates.

Consider fan-out loading of output A. The logic for each of the eight gates containing the A output is given in the left column of Table 13-7. The center column of this table shows the various bits of each gate for decimal number 7 stored in the counter ($A = 0, B = 1, C = 1, D = 1$). The right column of the table shows the fraction of the total gate current which output A sinks at this time.

Summation of the numbers in the right column yields the number 3¾. This indicates that current flow into output A is equal to 3¾ times the current of an

Table 13-7. Loading Conditions for Output A

Logic for gates containing A	Inputs for decimal number 7	Fraction of total gate current
$A\bar{B}\bar{C}\bar{D}$	0000	¼
$AB\bar{C}\bar{D}$	0100	⅓
$A\bar{B}C\bar{D}$	0010	⅓
$ABC\bar{D}$	0110	½
$A\bar{B}\bar{C}D$	0001	⅓
$AB\bar{C}D$	0101	½
$A\bar{B}CD$	0011	½
$ABCD$	0111	1

individual gate. As all possible combinations of B, C, and D are used in the table, output A conducts the above current whenever A is at the 0 state.

An analysis similar to the above is applied to the two-step decoder of Fig. 13-20 and shows that a flip-flop must sink a current which is equal to 5¼ times the current of a single gate. The gate load resistors can be increased in the two-step decoder in order to reduce the loading upon a flip-flop. However, the larger resistances will slow transient response of the decoder.

13-7. DECADE COUNTERS

Counters are often designed to recycle after every 10 input pulses. A counter of this type is referred to as a "decade counter." Decade counters may be cascaded so that the first counter counts to 10, the second counter counts to 100, and so on.

The decade counter may be derived from any of the counter configurations described in the preceding sections. Ten stages of the ring counter may be cascaded to provide an output signal after every ten input pulses. The cross-coupled feedback shift register becomes a decade counter when five flip-flops are connected in cascade. Modifications may also be made to the binary counter permitting it to be used as a decade counter. The following discussion pertains to use of the binary counter as a divide-by-10 network. This form of counter is referred to as a "binary decade counter."

A binary counter of n stages can be made to recycle after a count of fewer than 2^n input pulses. This is accomplished by using feedback to advance the state of the counter. In effect, one or more of the possible 2^n states is omitted. The minimum number of flip-flop stages to be used in a binary decade counter is four, as a three-stage binary counter cannot count beyond eight. If four stages are used, feedback signals eliminate six of the possible 16 states. It is possible, of course, to use five or more stages in a decade counter, but this would serve no useful purpose. Hence, the binary decade counters described below are implemented with four flip-flop stages.

There are various methods of forcing the four-stage binary counter to recycle after a count of ten. Figure 13-21 illustrates one of these methods. The true-output line of the last stage is capacitively coupled to pullover transistors in the

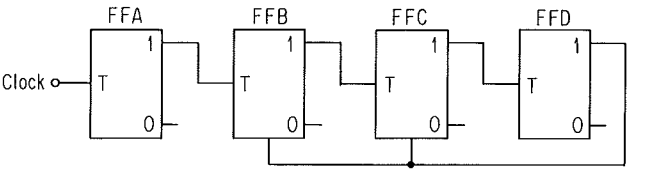

Fig. 13-21. Circuit connection in which output signal from last stage forces binary counter to recycle after 10 clock pulses.

second and third stages. When *FFD* changes to the 1 state, a positive-going signal is coupled back to *FFB* and *FFC*. This signal turns on the pullover transistors, and the latter two flip-flops are immediately switched to the 1 state. The circuit counts in normal fashion until the number 8 is reached. At this instant, the count changes from 0000 to 0001; the 0-to-1 transition of the last stage switches the second and third stages to the 1 state, so that the counter now stores 0111. A ninth clock pulse advances the counter to 1111, and the next clock pulse brings all stages to 0. Hence, the counter recycles after 10 input pulses.

Table 13-8 shows the counting sequence of the above counter, together with one possible set of decode logic for the 10 states. The four-stage Karnaugh map was used to obtain the various logic functions. A mapping of the 10 states shows that there are other sets of decode logic which can be implemented with the same number of diodes as the set listed in the table.

Although the circuit configuration of Fig. 13-21 is that of a sequential counter, the same feedback principle can be applied, without any circuit change, to the synchronous counter.

One other method of implementing a binary decade counter is shown by the synchronous connection of Fig. 13-22. When *FFD* is at the 0 state, the complementary output terminal of this stage is positive, and AND gate A_1 is able to pass the true-output signal of *FFA*. OR gate 0_1 permits the 0-to-1 transition of *FFC* to trigger *FFD* to the 1 state. The counter counts in normal fashion until the count 0001 (decimal number 8) is stored. The complementary output terminal

Table 13-8. Counting Sequence and Decode Logic for Binary Decade Counter of Fig. 13-21

Decimal number	True outputs $A\ B\ C\ D$	Decode logic
0	0 0 0 0	$\bar{A}\bar{B}\bar{C}$
1	1 0 0 0	$A\bar{B}\bar{C}$
2	0 1 0 0	$\bar{A}B\bar{C}$
3	1 1 0 0	$AB\bar{C}$
4	0 0 1 0	$\bar{A}\bar{B}C$
5	1 0 1 0	$A\bar{B}C$
6	0 1 1 0	$\bar{A}BC\bar{D}$
7	1 1 1 0	$ABC\bar{D}$
8	0 1 1 1	$\bar{A}BCD$
9	1 1 1 1	$ABCD$

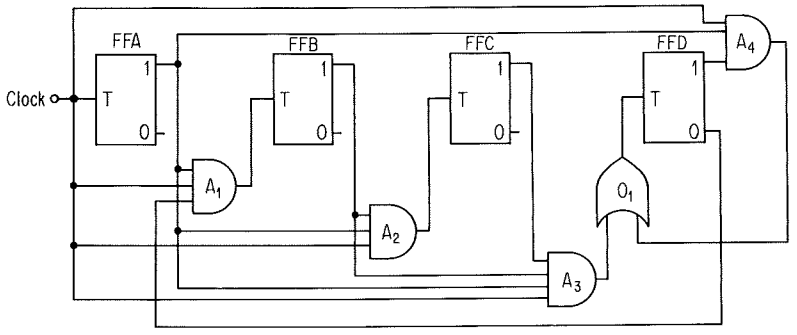

Fig. 13-22. Binary decade counter which utilizes output levels of *FFD* to steer output pulses from *FFA*.

of *FFD* is now at a low level, and gate A_1 is no longer able to couple pulses into *FFB*. The ninth input pulse advances *FFA* to the 1 state, and the counter stores 1001. When the clock pulse becomes positive for the tenth input pulse, AND gate A_4 is enabled and gate 0_1 couples a positive-level input signal to *FFD*. As the clock pulse falls to ground potential, *FFA* and *FFD* trigger to the 0 state; the counter now stores 0000 and has recycled.

13-8. COUNTING TO AN ARBITRARY LENGTH

Both the binary counter and the shift register can be made to recycle after a given number of input pulses. The preceding discussion showed how feedback is used to force the four-stage binary counter to recycle after 10 input pulses. This technique of applying feedback to omit certain combinations of stored variables can be used to obtain any desired cycle length for the n-stage binary counter (provided, of course, that the maximum count is not to be greater than 2^n).

Feedback is also applied to the shift register in order to obtain a desired cycle length.[8] A logical combination of variables stored in the register is applied to the inputs of the first stage; Fig. 13-23 shows a four-stage shift register having this type of feedback. The input logic, as well as the nature of the stored variables at time t_n, determines whether a 1 or 0 is to be stored in *FFA* at time t_{n+1}. The in-

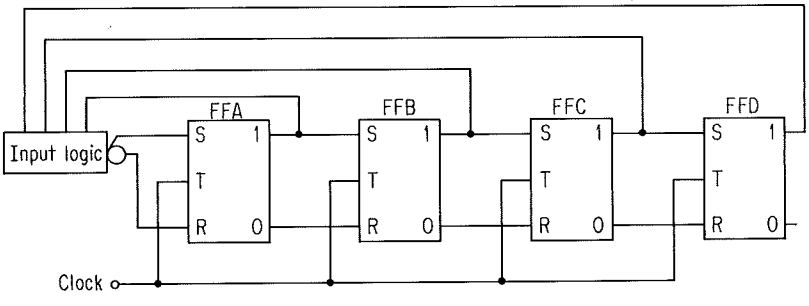

Fig. 13-23. Shift-register configuration for counting to an arbitrary length.

verted feedback signal to the reset input of *FFA* is necessary because the set and reset lines to a flip-flop must have opposite polarities. The Johnson counter described in Sec. 13-2 is a feedback shift register in which only the output of the last stage is fed back to the first stage; the NOT operation is performed on the feedback signal by cross-coupling the feedback lines.

Table 13-9. Sequence Table for Feedback Shift Register

Input pulse	True outputs *A B C D*
0	1 0 0 0
1	1 1 0 0
2	1 1 1 0
3	0 1 1 1
4	1 0 1 1
5	0 1 0 1
6	1 0 1 0
7	1 1 0 1
8	0 1 1 0
9	0 0 1 1
10	0 0 0 1
11	0 0 0 0

The n-stage shift register has 2^n possible combinations of individual states. Feedback can be used to obtain $2^n - 1$ of these states.[9] In other words, the feedback shift register is capable of counting to a number $2^n - 1$.

Except for the first stage, each stage of the shift register must successively store the bit which was previously stored in the preceding stage. Consequently, a tabulation of all successive bits stored in *any* stage can be used to determine the state of each stage at any given time. This technique is used in counter design.

As an example of counter design, consider that a feedback shift register is to count to 12. The flip-flops used are considered to be either the trigger type or the master-slave type, where a master-slave *pair* is considered as a single flip-flop. A minimum of four flip-flop stages is required to provide the desired count. Let the resulting counter contain four flip-flops, designated as *FFA*, *FFB*, *FFC*, and *FFD*. Shifting is from left to right, so that *FFA* and *FFD* are the input and output stages, respectively.

Arbitrarily select a sequence of output bits for the last stage; let this sequence be 000111010110, where time progresses to the *right.* From this sequence, the listing of Table 13-9 is obtained. The various true outputs of *FFD* correspond to the above sequence written in a vertical fashion (because time progresses from top to bottom in the table). As the bit stored in *FFD* at time t_n was stored in *FFC* at time t_{n-1}, the true outputs of *FFC* are obtained by shifting each bit from column *D* up by one pulse position and placing it in column *C*. The first bit in column *D*, a 0 in this case, is placed at the bottom of column *C*. A similar procedure is used to write the sequences for *A* and *B*.

Feedback logic to the input of *FFA* is determined from Table 13-9. For each input pulse where a 1 is stored in *FFA*, the bits stored in the register for the *previous* input pulse determine the feedback logic to provide the 1. For instance, a 1 is stored in *FFA* by the 0 input pulse; for the previous input pulse (pulse 11), the stored bits are 0000. Consequently, the feedback logic must be

$$f_0 = \bar{A}\bar{B}\bar{C}\bar{D} \tag{13-14}$$

in order to provide a 1 to *FFA* for the 0 input pulse. Combining the individual feedback expression yields

$$f = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} + \bar{A}BCD + \bar{A}B\bar{C}D + A\bar{B}CD \tag{13-15}$$

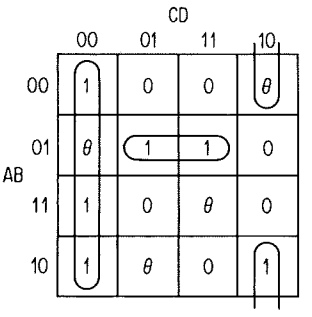

Fig. 13-24. Karnaugh map plot of Eq. (13-15).

This last expression can be plotted on the Karnaugh map, together with the optional terms. Figure 13-24 shows the resulting plot and indicates the manner in which cubes may be combined to provide a simplified logic expression. The resulting feedback logic becomes

$$f = \bar{A}BD + \bar{B}C\bar{D} + \bar{C}\bar{D} \qquad (13\text{-}16)$$

It has been assumed that the above register will never contain the four optional terms plotted on the map. However, suppose that any one of these terms is stored during the initial application of supply voltage to the circuit. The question which now arises is "Will the counter cycle to one of the terms in Table 13-9?" Inspection of counter operation reveals that the counter will eventually advance to a suitable count. Each of the four optional terms is alternately assumed to be stored in the counter. The optional term 0010 cycles to 1001, 0100, and 1010. As this last term is contained in Table 13-9, the counter now advances in normal fashion. Three input pulses are required to put the counter in the correct count sequence for the above optional term; fewer input pulses are required if any one of the other three optional terms is initially stored in the register.

The Karnaugh map can also be used to determine decode logic for the 12 output states of the above counter. This procedure is similar to that described earlier in conjunction with the binary decade counter.

The above discussion has shown that various patterns of ones and zeros may be obtained at any output terminal of a feedback shift register. This pattern may be selected so as to appear almost random in nature. Hence, the feedback shift register may be used as a pseudo-random pulse generator.

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14

Pulse-generating and Pulse-shaping Networks

14-1. MONOSTABLE (ONE-SHOT) MULTIVIBRATORS

Two inverter stages can be connected as shown in Fig. 14-1 to provide a single output pulse each time an input pulse occurs. The base of transistor Q_1 is dc-coupled to the collector of transistor Q_2, whereas the base of Q_2 is ac-coupled *only* to the collector of Q_1. During steady-state conditions, Q_2 is turned on by current flow through resistor R_1, and V_{out} is close to ground potential. There is no forward base drive to Q_1, and this device is turned off. Capacitor C_1 charges through resistor R_2 and the base-emitter diode of Q_2; this capacitor charges to the level $V_{CC} - V_{BE(ON)}$ (neglecting the small voltage drop across R_2, as a result of collector leakage current). When an input pulse is applied to capacitor C_2, the pulse is differentiated and appears at the anode of diode D_1 as either a positive- or a negative-voltage spike. A positive-voltage spike forward-biases Q_1, and this transistor becomes saturated. The left side of C_1 now falls to a $V_{CE(sat)}$ level; as voltage across C_1 cannot change instantaneously, the base of Q_2 becomes negative by the amount $V_{CC} - V_{BE(ON)} - V_{CE(sat)}$. This negative base voltage turns Q_2 off, and collector voltage of Q_2 rises to a positive level. Forward base drive is now applied to Q_1 through resistor R_3, and this latter transistor is held on. Base voltage of Q_2 does not remain negative indefinitely, as C_1 is connected through R_1 to a positive supply voltage. Hence, immediately upon turnoff of Q_2, C_1 begins charging through R_1 and the collector-emitter conduction path of Q_1; the right side of C_1 now rises toward the level $V_{CC} - V_{CE(sat)}$. However, when base voltage of Q_2 rises to approximately 0.65 volt, this device turns on; forward base drive is

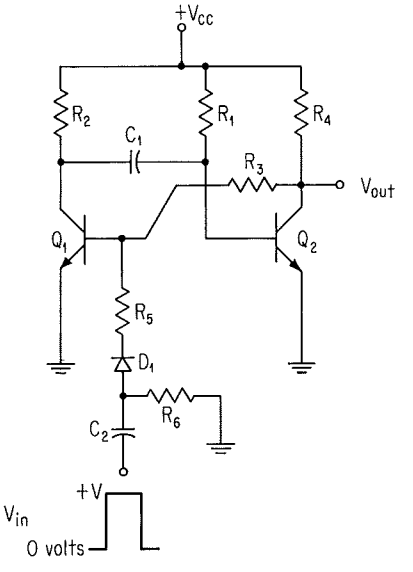

Fig. 14-1. Circuit configuration of monostable multivibrator.

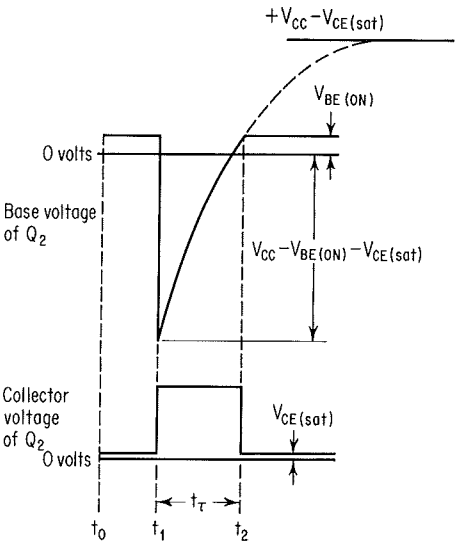

Fig. 14-2. Base- and collector-voltage waveforms for Q_2 in Fig. 14-1.

removed from Q_1, and this latter transistor turns off. The circuit is now at its steady-state condition, and C_1 again charges to the level $V_{CC} - V_{BE(ON)}$.

The purpose of diode D_1 in Fig. 14-1 is to prevent a negative-going input voltage from turning Q_1 off. This diode should have a fast recovery time; otherwise, a negative spike may be transmitted to the base of Q_1. If a negative spike does appear at the base of Q_1, the output pulse can be no wider than the input pulse.

From the preceding discussion it is clear that the circuit of Fig. 14-1 has one *stable* state and one *quasi-stable* state. The circuit is a form of *monostable* multivibrator; it is generally referred to as a "single-shot multivibrator," or as a "one-shot." The term one-shot is used here.

Output voltage of the one-shot in Fig. 14-1 is normally near ground potential and rises to a positive level upon application of a positive-going input signal. Duration of the positive-level output signal is determined by the time required for C_1 to charge to the base-emitter turn-on voltage of Q_2. This charging time is determined principally by the maximum negative voltage applied to the base of Q_2 and also by the product R_1C_1.

Figure 14-2 shows waveforms for base voltage and collector voltage of Q_2 in the circuit of Fig. 14-1. At time t_0, Q_2 is saturated, and base voltage of this device is at the $V_{BE(ON)}$ level; also, collector voltage of Q_1 is at a $V_{CE(sat)}$ level. The circuit is switched to the unstable state at time t_1, and base voltage of Q_2 becomes negative.* Collector voltage of Q_2 now rises to a positive level. As time advances from the t_1 point, base voltage of Q_2 rises toward a positive level and becomes clamped, at time t_2, to the $V_{BE(ON)}$ level of Q_2; collector voltage of Q_2 now falls to the $V_{CE(sat)}$ level. The dashed portion of the base-voltage curve shows the path along which C_1 would charge if the above clamping action did not occur. Output voltage of the circuit is at a positive level for the time interval t_τ.

* It is presently assumed that the base-emitter diode of Q_2 can withstand the negative-voltage level shown.

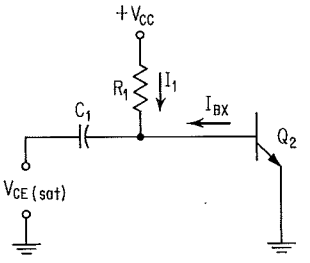

Fig. 14-3. Charging circuit for C_1 in Fig. 14-1; Q_2 is at cutoff, and Q_1 is in saturation.

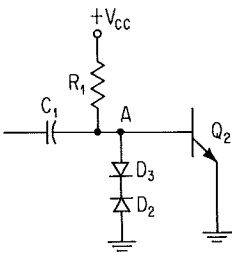

Fig. 14-4. Use of two diodes to clamp reverse base voltage of Q_2.

During the t_τ time interval in Fig. 14-2, C_1 is charged by current flow through R_1 and by base reverse-leakage current I_{BX} of Q_2. Figure 14-3 shows the present charging circuit for C_1. The effect of I_{BX} is to charge C_1, through R_1, from an equivalent voltage source $V_{CC} + I_{BX}R_1$.[1] However, as the product $I_{BX}R_1$ is generally small, this component of charging voltage is neglected.* Beginning at time t_1, voltage at the base of Q_2 is described by

$$V_{B2} = V_{CC} - (2V_{CC} - V_{BE(ON)} - V_{CE(sat)})e^{-t/R_1C_1} \tag{14-1}$$

where V_{B2} = base voltage of Q_2
t = time greater than t_1
At time t_2, V_{B2} rises to the level $V_{BE(ON)}$; hence t_τ is given by

$$t_\tau = R_1C_1 \ln \frac{2V_{CC} - V_{BE(ON)} - V_{CE(sat)}}{V_{CC} - V_{BE(ON)}} \tag{14-2}$$

If base-emitter reverse breakdown voltage $V_{(BR)EBO}$ of Q_2 in Fig. 14-1 is smaller than the magnitude of $V_{CC} - V_{BE(ON)} - V_{CE(sat)}$, the negative excursion of base voltage in Fig. 14-2 is clamped to the $V_{(BR)EBO}$ level. The expression for t_τ then becomes

$$t_\tau = R_1C_1 \ln \frac{V_{CC} + V_{(BR)EBO}}{V_{CC} - V_{BE(ON)}} \tag{14-3}$$

The transistor data sheet generally specifies a minimum value for $V_{(BR)EBO}$, although the actual value for a particular device may be somewhat above this minimum breakdown level. In order to assure a *known* level of most negative base voltage to Q_2, two diodes are often connected across the base-emitter junction of Q_2, as shown in Fig. 14-4. When voltage at point A is positive, diode D_2 is reverse-biased; consequently, there is no "robbing" of forward base current to Q_2. Diode D_3 is a low-voltage breakdown diode. A negative-going voltage at point A is clamped by D_3 and D_2 to the *sum* of the breakdown voltage of D_3 and the forward diode drop of D_2. This voltage level should be lower than $V_{(BR)EBO}$ of Q_2, and is substituted for $V_{(BR)EBO}$ in Eq. (14-3).

* All transistor leakage currents are neglected in the present transient analysis. This is justified by the argument that variation of $V_{BE(ON)}$ and $V_{CE(sat)}$ levels among various transistors is generally greater than the effects of transistor leakage currents.

A base speedup capacitor is generally connected across R_3 in Fig. 14-1. This capacitor improves transient response of Q_1 and gives the circuit a faster transition time from one state to the other; in addition, the circuit becomes easier to trigger. (The discussion of Sec. 6-7 gives typical values of speedup capacitance for various transistor types.)

Two charging intervals are associated with C_1 in the one-shot circuit of Fig. 14-1. One of these intervals—the time required for base voltage of Q_2 to charge from a maximum negative level to a $V_{BE(ON)}$ level—is described by Eq. (14-2) or (14-3). The second charging interval begins when the circuit switches to its stable state; C_1 now charges through R_2 to the $V_{CC} - V_{BE(ON)}$ level.

If the circuit is triggered to its quasi-stable state before C_1 becomes fully charged, base voltage of Q_2 does not decrease to the negative level shown in Fig. 14-2, and the t_τ value becomes smaller than that given by Eq. (14-2). The time required to charge C_1 fully is designated "recovery time" t_{rr} of the one-shot. A useful rule of thumb is to allow three time constants for t_{rr}; hence, t_{rr} can be expressed

$$t_{rr} = 3R_2C_1 \tag{14-4}$$

Maximum repetition rate R_M of the one-shot is determined by the *sum* of t_τ and t_{rr}; thus

$$R_M = \frac{1}{t_\tau + t_{rr}} \tag{14-5}$$

A pullover transistor is often used in place of the input diode D_1 in Fig. 14-1. This transistor is driven from the external pulse source and serves to switch the circuit to its quasi-stable state. Figure 14-5 shows the one-shot implemented with pullover transistor Q_3; this circuit also includes a speedup capacitor C_2 and the two series diodes for limiting reverse base voltage to the output transistor. When Q_3 turns on, the negative-going collector voltage of this device switches the circuit to its quasi-stable state. If Q_3 is turned off during the quasi-stable interval, there is no effect upon circuit operation, as transistor Q_1 is on and maintains the left side of C_1 at a $V_{CE(sat)}$ level.

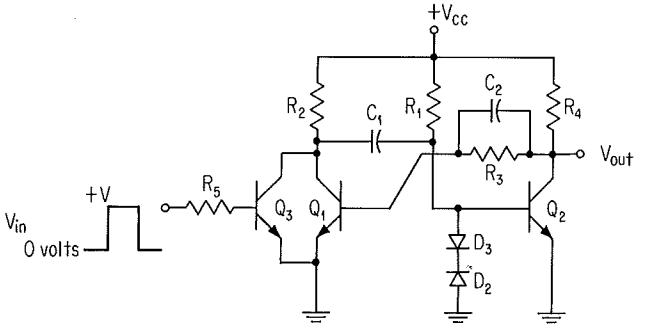

Fig. 14-5. One-shot circuit incorporating pullover transistor Q_3, speedup capacitor C_2, and diode clamp.

One application of the one-shot is as a pulse-shaping network; amplitude and duration of the output pulse may be made independent of the input-voltage waveform. The circuit is often used to generate pulses of fixed amplitude and duration.

The trailing edge of a one-shot may be inverted and used to trigger a second one-shot; the output pulse of the second one-shot is thus delayed by the width of output pulse from the first one-shot. The first one-shot serves as a *delay* element in this application.

A typical design example for the one-shot is presented below.

EXAMPLE 14-1

PROBLEM: Design a one-shot which is to be triggered by the leading edge of a +3-volt, 100-nsec-wide input pulse. The positive-level output pulse is to be 200 μsec wide and at least +3.5 volts for a current of 1 ma into an external load. A supply voltage of +6 volts is to be used.

SOLUTION: *Step 1.* The circuit is implemented with N-P-N transistors to meet the positive-level trigger requirement. These transistors are diffused-base devices, in order to be triggered by a 100-nsec-wide pulse. The 2N3014 (N-P-N epitaxial silicon) transistor is used.

Step 2. As the output pulse is to be wider than the input pulse, a pullover transistor is used at the input.

Step 3. The 2N3014 transistor has a minimum $V_{(BR)EBO}$ rating of −5 volts. Consequently, during the quasi-stable circuit condition, the negative excursion of base voltage to the OFF transistor may be restricted to this −5 volts level. In order to assure a *known* level of most negative base voltage, two diodes are connected to the base of the output transistor, as shown in Fig. 14-4. Diode D_3 is a 3.9-volt breakdown diode (1N748), and diode D_2 is a general-purpose diode (such as the 1N645) having a nominal forward-voltage drop of 0.65 volt. These two diodes limit negative base voltage to approximately −4.55 volts.

Step 4. The above three steps indicate that the circuit configuration of Fig. 14-5 is to be used. According to the circuit specifications, 1 ma of current flows from the collector of Q_2 when the circuit is at its stable state; V_{out} must be at least +3.5 volts during this time. Hence, voltage drop across resistor R_4 can be no larger than 2.5 volts when Q_2 is at cutoff. If collector reverse-leakage current of Q_2 and base current to Q_1 are neglected, R_4 can have a maximum value of 2.5 kilohms. Let R_4 tentatively be 1.5 kilohms for the circuit.

Step 5. ON-state collector current of Q_2 is equal to $(V_{CC} - V_{CE(\text{sat})})/R_4$, or approximately 3.9 ma. According to the 2N3014 data sheet, a minimum h_{FE} of 25 is guaranteed when I_C has a level of 10 ma. Let us assume that h_{FE} has a minimum value of 20 at the 3.9-ma level for I_C. The circuit is to be designed for a forced gain of $0.4h_{FE}$. Hence, forward base current to Q_2 is described by

$$I_{B1} = \frac{2.5I_C}{h_{FE}} \tag{14-6}$$

Forward base current of Q_2 can also be expressed

$$I_{B1} = \frac{V_{CC} - V_{BE(\text{ON})}}{R_1} \tag{14-7}$$

Equations (14-6) and (14-7) can be solved for R_1 to yield

$$R_1 = \frac{(V_{CC} - V_{BE(\text{ON})})h_{FE}}{2.5I_C} \tag{14-8}$$

With the exception of $V_{BE(\text{ON})}$, all values on the right side of Eq. (14-8) are known. Substitution of the known values into this expression, together with a nominal value of 0.65 volt for $V_{BE(\text{ON})}$, gives a value of 11 kilohms for R_1.

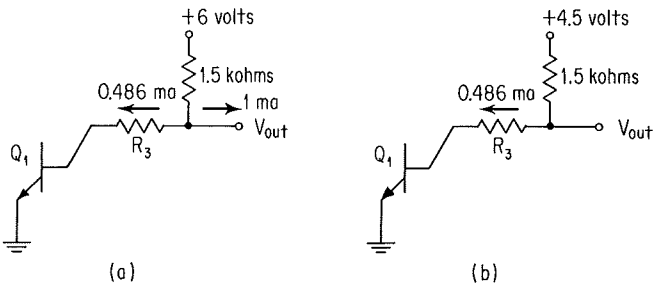

Fig. 14-6. Input dc circuits for Q_1 in Fig. 14-5; Q_2 is at cutoff. *(a)* **complete circuit;** *(b)* **equivalent circuit to show effect of 1 ma load current.**

Step 6. Capacitor C_1 is determined from Eq. (14-3), where the value 4.55 volts is substituted for $V_{(BR)EBO}$. This calculation gives a value of 0.062 μf for C_1.

Step 7. As there is no specification for maximum repetition rate of the one-shot, resistor R_2 can be arbitrarily selected. Let this resistor have the same value as R_4, or 1.5 kilohms.

Step 8. Transistors Q_1 and Q_2 have identical ON-state collector loading. Consequently, both devices should have the same forward base current. From Eq. (14-7), this current is determined to be 0.486 ma. For Q_2 at cutoff, the approximate dc input circuit to the base of Q_1 is shown in Fig. 14-6*a*; collector leakage current of Q_2 is small and is neglected. Figure 14-6*b* shows the equivalent circuit for calculating the positive-level output voltage V_{out} and also R_3. The V_{out} level is determined to be +3.7 volts; this value is larger than the specified +3.5-volt minimum level. Consequently, the 1.5-kilohm value for R_4 is suitable. A value of 6.43 kilohms is calculated for R_3.

Step 9. Resistor R_5 is to provide a forward base current of 0.486 ma to Q_3 when V_{in} is at the +3-volt level. This resistor is determined to have a value of 4.84 kilohms.

Step 10. The exact value of C_2 is unimportant. From the discussion of Sec. 6-7, C_2 is chosen to have a value of 20 pf.

DISCUSSION: A tentative value for R_4 was selected in step 4. The calculation of V_{out} in step 8 indicated that for Q_2 at cutoff, total current flow through R_4 gives a V_{out} level which is greater than the desired level of +3.5 volts. Hence, the tentative value for R_4 was suitable.

14-2. ASTABLE (FREE-RUNNING) MULTIVIBRATORS

Let two inverter stages be cross-coupled as shown in Fig. 14-7. The circuit configuration is that of two transistors which are ac-coupled only to each other. From the preceding analysis of one-shot operation, it is apparent that the circuit has *two* quasi-stable states. Consider that transistor Q_1 has just switched from cutoff to saturation. The negative-going voltage level at the collector of this device is transmitted, through capacitor C_1, to the base of transistor Q_2. This latter transistor is biased to cutoff until C_1 charges through resistor R_2 to the $V_{BE(ON)}$ level of Q_2. At this instant, Q_2 turns off, and Q_1 turns on. Further analysis will show that Q_1 remains off for a fixed time interval, and then turns on. The above cycle is repeated indefinitely. This circuit is an *astable* multivibrator; it is com-

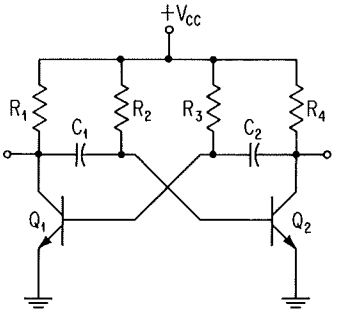

Fig. 14-7. Circuit of astable, or free-running, multivibrator.

monly referred to as a "free-running multivibrator," or, more simply, as a "multivibrator." The name free-running multivibrator is used here.

Considerations regarding the negative-level base-input signal to the one-shot were discussed in Sec. 14-1. These same considerations apply also to the negative-level base-input signals to the free-running multivibrator; hence, Eqs. (14-2) and (14-3) (modified, of course, to include the correct RC product) are applicable to the free-running multivibrator. If diodes are used at the base of a transistor as in Fig. 14-4, the $V_{(BR)EBO}$ term in Eq (14-3) is replaced by the *total* diode drop for a negative-voltage level (as was done in the example of Sec. 14-1). The period of oscillation of a free-running multivibrator is equal to the *sum* of the t_τ intervals calculated for each transistor. If both halves of the circuit are identical, each output-voltage waveform is symmetrical, i.e., each has a 50 per cent duty cycle. By selecting unequal RC time constants for the two transistor bases, each output-voltage waveform may be made unsymmetrical.

Output signals appear at the collectors in Fig. 14-7. When a transistor turns on, collector voltage of the device falls quickly to a $V_{CE(\text{sat})}$ level. However, when this same transistor turns off, collector voltage increases only as fast as capacitance at the collector terminal can be charged through the collector-load resistance. This capacitance is the parallel combination of the cross-coupling capacitance, transistor output capacitance, and external-load capacitance. Generally, the cross-coupling capacitance is considerably larger than the sum of the other two capacitances.

From the above discussion, it is evident that t_f (fall time) of an output-voltage waveform is larger than t_r (rise time) in the circuit of Fig. 14-7.* One excellent method of improving t_f is by the addition of two diodes and two resistors as shown in Fig. 14-8.[2] Diodes D_1 and D_2, as well as resistors R_5 and R_6, have been added to the basic circuit of Fig. 14-7. When transistor Q_1 turns off, capacitor C_1 charges through resistor R_5. Diode D_1 prevents resistor R_1 from supplying charging current to C_1. Consequently, collector voltage of Q_1 is able to rise quickly to a highly positive level. A similar analysis shows that collector voltage of Q_2 rises quickly to a highly positive level when this latter device turns off. The present circuit configuration is capable of reducing t_f by a factor of 10, as compared to the free-running multivibrator circuit of Fig. 14-7.

* See the discussion of Sec. 4-5 for definitions of t_f and t_r.

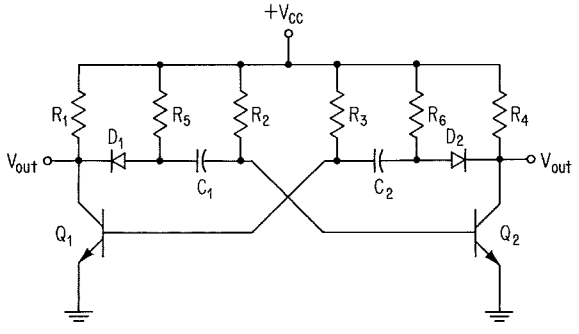

Fig. 14-8. Circuit configuration to reduce t_f of free-running multivibrator.

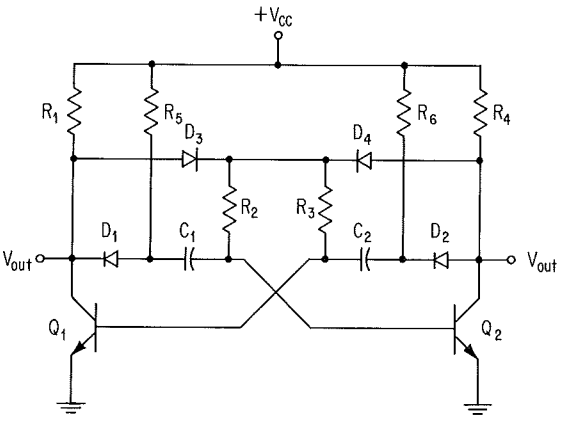

Fig. 14-9. Self-starting, free-running multivibrator.

The two free-running multivibrator circuits described above are not necessarily self-starting. In some instances, the two cross-coupled transistors may saturate upon the initial application of supply voltage. If this does occur, both devices remain in the saturated state indefinitely.

A free-running multivibrator which has a self-starting feature is shown in Fig. 14-9.[2] This latter circuit is similar to that of Fig. 14-8 except that resistors R_2 and R_3 are no longer connected to $+V_{CC}$ but instead are coupled through diodes D_3 and D_4 to the collectors of Q_1 and Q_2.

As base drive to a conducting transistor must now flow through the collector load resistor of the OFF device, it is not possible for both transistors to saturate simultaneously. This circuit retains the feature of a fast t_f for the output-voltage waveform.

14-3. GENERATION OF VARIOUS COMBINATIONS OF PULSES

The discussion of Sec. 13-8 pointed out that the feedback shift register can be used to generate various combinations of pulses. Pulse sequences of this nature can also be obtained by combining various switching and logic circuits. Figure 14-10 shows a block diagram of a system which performs this latter function. Input pulse train ϕ triggers a flip-flop and serves as one input to an AND gate. An output signal from the flip-flop is also applied to the AND gate. Consequently, the output of this logic gate has the same pulse width as the ϕ signal but at one-half the repetition rate. Thus, every second pulse has been removed from the ϕ pulse train.

Additional flip-flops and logic circuitry can be incorporated into the above system, permitting many different combinations of pulses to be derived from the ϕ pulse train.

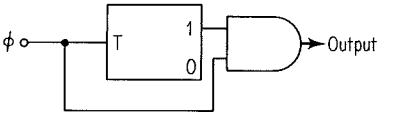

Fig. 14-10. Circuit for providing pulses at one-half repetition rate of ϕ pulse.

REFERENCES

1. Millman, J., and H. Taub: "Pulse, Digital, and Switching Waveforms," chap. 11, McGraw-Hill Book Company, New York, 1965.
2. Mattox, W. J., II: High Square, Variable Frequency Multivibrator, *Electron. Equipment Eng.*, p. 35, July, 1961.

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